ACQ400-MTCA-RTM-2

2 Site Carrier for MTCA RTM

Product Description

- 2 Site D-TACQ FMC/ELF RTM Module.
- Compatible with DAMC-FMC1Z7IO AMC Module.
- Compatible with KMCUZ30 AMC Module.
- MTCA.4 compliant, mid-size, double-width µRTM module.
- Zone 3 Class D1.0 RTM Connector to AMC.
- Includes analogue power supplies for ELF modules.

Key Features

- Provides 2 sites of D-TACQ ELF modules giving up to 64 channels Analog Inputs.
- Compatible with the majority of D-TACQ ELF and FMC Modules.
- 2x ADF-30 / ZD30 hard metric differential connectors to front side card.
  - Pinout compliant with D1.0 DESY Zone 3 Recommendation (Rev A.3).
  - Pinout allows connectivity with all D-TACQ ULPC and DLPC modules. Includes I^2C interface to read ELF PROMS and control analogue and digital PSUs.

Platform Key Features

D-TACQ supplies a complete working Intelligent Digitizer Appliance providing:

- FPGA based system with a range of flexible and customisable features.
- Microprocessor system running open source Linux.
- Comprehensive API provided in Python.
- Onboard EPICS IOC for rapid integration.

Please contact info@d-tacq.com for details on the above system integration options.

Figure 1: Board Photo

Rev 1 November 2024

sales@d-tacq.com
www.d-tacq.com

Table Of Contents

0.1 Glossary

- FMC: VITA57 FPGA Mezzanine Card
- Xilinx ZYNQ: System-on-chip Dual core ARM microprocessor + FPGA logic
- LPC: FMC Low pin count wiring standard
- ELF: Superset mechanical/electrical variant of FMC (D-TACQ FMC variation)
- ULPC: FMC Ultra low pin count (D-TACQ FMC variation)
- DLPC: FMC Differential low pin count(D-TACQ FMC variation)
- MP: Management Power (MTCA.4 term)
- SPL: Single Pin Lemo Connector

0.2 Applicable Specifications

- MTCA.0
- AMC.0
- MTCA.4
- D1.0 DESY Zone 3 Recommendation (Rev A.3)
- Management Interface IPMI v2.0

1 Product Description

1.1 Applications

Instrumentation applications, control and monitoring.

1.2 Overview

- Micro TCA [See Section 0.2] provides an instrument data acquisition platform with high bandwidth connections using fast serial buses, and standardised platform management using IPMI.
- Micro TCA Extensions for Physics [See Section 0.2] provides for a µRTM module that allows expansion for a processor card or adc module on the front side.
- The FMC standard [See Section 0.2] provides for low cost IO expansion to an FPGA processor module. D-TACQ provides a range of modules that extend this standard in two ways – the “ELF” [See Section 0.1] module, which more than doubles the payload of the module and the “ULPC” [See Section 0.1]and “DLPC” [See Section 0.1] pinouts that define a subset of IO’s suitable for relatively low speed modules (up to 200MBytes/sec) and, in addition provide for analogue power rails from the baseboard. D-TACQ designs and markets a range of FMC and ELF modules, where the ELF modules in particular enable both high channel density and high analogue quality in the module.
- This document defines a MTCA.4 compliant µRTM that can act as a carrier for 2 x ELF modules. The µRTM is dependent on a suitable front side AMC module, similar to DAMC-FMC1Z7IO.

1.3 Module Compatibility

The ELF module standard is a D-TACQ standard and is compatible with only D-TACQ Carriers.
The DAMC-FMC1Z7IO-RTM-2 supports the D-TACQ ELF Module Standard and also FMC modules manufactured by D-TACQ . All D-TACQ Modules are supported apart from the alternative front panel BLF modules.

3rd party FMC may be compatible provided the I/O used on the module matches the subset of the full I/O available on the ELF carrier.

Please contact info@d-tacq.com for details on module support for the RTM.

Details of D-TACQ modules can be found at D-TACQ Modules .

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

2 Physical

2.1 µRTM Compliance

- ACQ400-MTCA-RTM-2 is an MTCA.4 compliant, mid-size, double width µRTM module.
- The ZONE 3 connector is be compatible with the DESY MTCA.4 D1.0 Zone 3 recommended specification see Section. 0.2
- RTM Front Panel (MTCA Rear Panel) allows for 2 x standard FMC front panels and a single input ”Clock” signal see Section 4.3

2.2 Board Appearance

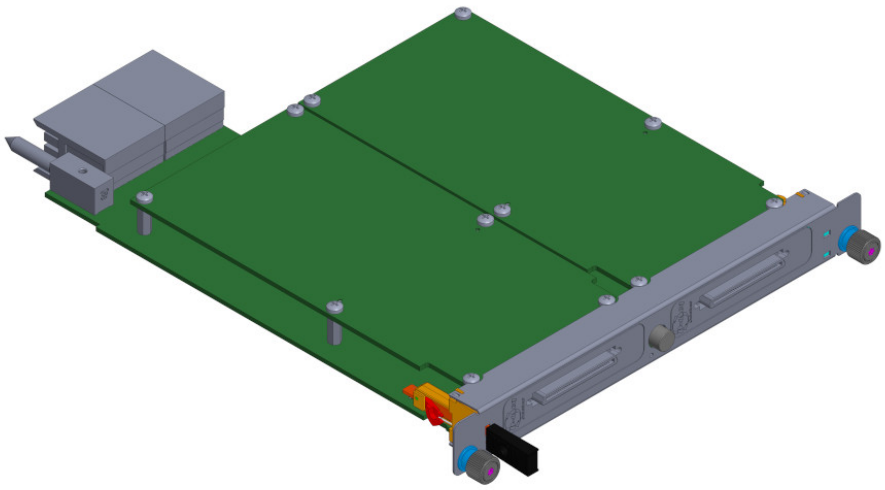


Figure 2: Board Appearance

3 AMC Interface

3.1 Zone 3 Connectors

ACQ400-MTCA-RTM-2 is fitted with connectors as specified by AMC.0 and MTCA.4. These are TE Connectivity 6469183-1 connectors.

Mating connectors for the AMC board should be compatible, for example the TE Connectivity 6469081-1 connectors.

3.2 Zone 3 Signaling Levels

JTAG and standard MMC I^2C lines operate at +3.3V logic levels.

Although the majority of ELF1 and ELF2 signals are routed as differential pairs, many of the ELF modules only use these as single-ended traces.

D-TACQ ELF modules work optimally at +1.8V voltage levels but can also support +2.5V. The ELF FPGA I^2C buses also work optimally at +1.8V logic levels.

The RTM Front Panel (MTCA Rear Panel) clock (output from RTM, input to AMC) is at LVDS signaling levels.

3.2.1 Differential Pairs Polarity Definition

There appears to be a small mistake in version A.3 of the D1.0 specification. MTCA.4 REQ 2-27 states for differential signal pairs, signals A, C and E shall be assigned as positive (+) and B, D and F as negative (-). However the pin names in Table 1 and Table 2 label both signals A/B and E/F as positive in some, but not all cases. We have proceeded under the assumption that this was a typographical error but have noted where the ACQ400-MTCA-RTM-2 pin name differs.

3.2.2 VADJ Potential Voltage Mismatch Issue

The D1.0 specification does not provide a hardware mechanism for the AMC card to provide/determine the signaling voltage used by the µRTM. This voltage is currently required to be generated by both cards.D-TACQ has made provision for this to be provided on the AMC card to the µRTM to power the I/O supplies of any ELF modules. This is similar to the way an FMC/ELF card receives its $+V_{FMCIO}$ voltage from the carrier. If implementation is desired, spare pins which could potentially be used for this supply voltage are shown in Table 2. This voltage will require to supply a maximum current of 300mA as this is the maximum $+V_{FMCIO}$ current that 2 ELF modules will require.

This is a non-standard change and is only supported on specific AMCs such as the DAMC-FMC1Z7IO please contact info@d-tacq.com for details. This AMC has these lines connected via resistor jumpers to allow an AMC card to be fully DESY D1.0 compliant.

3.3 Zone 3 Connector Pinouts

3.3.1 RP30

The RP30 connector conforms to the D1.0 DESY Zone 3 Recommendation.
The Table below gives the pin number mapping from the D1.0 pin naming to the ELF(as per FMC convention) pin names as used by the ELF1 and ELF2 connectors.

Pin	Pin Name (DESY D1.0)	Function Name	Description
A1	PWRA1	+12V	µRTM-PWR Payload Power +12V
B1	PWRB1	+12V	µRTM-PWR Payload Power +12V
A2	PWRA2	+12V	µRTM-PWR Payload Power +12V
B2	PWRB2	+12V	µRTM-PWR Payload Power +12V
A3	AMC_CLK1+	NC	
B3	AMC_CLK1-	NC	
A4	AMC_TCLK+	NC	
B4	AMC_TCLK-	NC	
A5	P30_IO+/CC	ELF2_LA01_CCp	
B5	P30_IO-/CC[1]	ELF2_LA01_CCn	
A6	P30_IO+/CC	ELF2_LA00_CCp	
B6	P30_IO-/CC[1]	ELF2_LA00_CCn	
A7	P30_IO+	ELF2_LA18_CCp	
B7	P30_IO-	Reserved (ELF2_SDA)	ELF2 I^2C Data +3.3V Logic
A8	P30_IO+	ELF2_LA15p	
B8	P30_IO-	Reserved (ELF1_SCL)	ELF1 I^2C Clock +3.3V Logic
A9	P30_IO+/CC	ELF2_CLK0_M2Cp	
B9	P30_IO-/CC[1]	ELF2_CLK0_M2Cn	
A10	P30_IO+/CC	ELF1_LA01_CCp	
B10	P30_IO-/CC[1]	ELF1_LA01_CCn	
C1	PS	Present	Present - connected to GND.
D1	SDA	SDA I^2C Data	+3.3V Logic
C2	MP	+3V3_MP	µRTM-MP Management Power +3V3
D2	SCL	SCL	I^2C Clock +3.3V Logic
C4	OUT0+	ELF1_CLK1_C2Mp	ELF1 Carrier to Mezzanine Clock
D4	OUT0-	ELF1_CLK1_C2Mn	ELF1 Carrier to Mezzanine Clock
C5	P30_IO+	ELF2_LA23p	
D5	P30_IO-	ELF2_LA22p	
C6	P30_IO+	ELF2_LA20p	
D6	P30_IO-	I^2C_SCL_1V8	FPGA I^2C Clock +1.8V Logic [4.2]
C7	P30_IO+	ELF2_LA17_CCp	
D7	P30_IO-	Reserved (ELF2_SCL)	ELF2 I^2C Clock +3.3V Logic
C8	P30_IO+	ELF2_LA14p	
D8	P30_IO-	NC	
C9	P30_IO+	ELF2_LA12p	
D9	P30_IO-	NC	
C10	P30_IO+	ELF2_LA10p	
D10	P30_IO-	ELF2_LA10n	
E3	OUT2+	NC	
F3	OUT2-	NC	
E4	OUT1+	ELF2_CLK1_C2Mp	ELF2 Carrier to Mezzanine Clock
F4	OUT1-	ELF2_CLK1_C2Mn	ELF2 Carrier to Mezzanine Clock
E5	P30_IO+	ELF2_LA21p	
F5	P30_IO-	I^2C_SDA_1V8	FPGA I^2C Data +1.8V Logic [4.2]
E6	P30_IO+	ELF2_LA19p	
F6	P30_IO-	I^2C_RESETn	Reset line for I^2C Bus Splitter +1.8V Logic [4.2]
E7	P30_IO+/CC	ELF2_LA16p	
F7	P30_IO-/CC[1]	Reserved (ELF1_SDA)	ELF1 I^2C Data +3.3V Logic
E8	P30_IO+/CC	ELF2_LA13p	
F8	P30_IO-/CC[1]	NC	
E9	P30_IO+	ELF2_LA11p	
F9	P30_IO-	ELF2_LA11n	
E10	P30_IO+	ELF2_LA09p	

[1] Polarity issue in version A.3 of the D1.0 specification,[See Section 3.2.1].

Table 1: J30 RTM Connector Pinout

3.3.2 RP31

The RP31 connector conforms to the D1.0 DESY Zone 3 Recommendation.
The Table below gives the pin number mapping from the D1.0 pin naming to the ELF(as per FMC convention) pin names as used by the ELF1 and ELF2 connectors.

Pin	Pin Name (DESY D1.0)	Function Name	Description
A1	P31_IO+	ELF2_LA08p	
B1	P31_IO-	ELF2_LA08n	
A2	P31_IO+	ELF2_LA05p	
B2	P31_IO-	ELF2_LA05n	
A3	P31_IO+/CC	ELF2_LA02p	
B3	P31_IO-/CC[1]	ELF2_LA02n	
A4	P31_IO+/CC	ELF1_LA20p	
B4	P31_IO-/CC	NC	
A5	P31_IO+	ELF1_LA17_CCp	
B5	P31_IO-	NC	
A6	P31_IO+	ELF1_LA14p	
B6	P31_IO-	NC	
A7	P31_IO+/CC	ELF1_LA00_CCp	
B7	P31_IO-/CC[1]	ELF1_LA00_CCn	
A8	P31_IO+/CC	ELF1_CLK0_M2Cp	
B8	P31_IO-/CC[1]	ELF1_CLK0_M2Cn	
A9	P31_IO+	ELF1_LA07p	
B9	P31_IO-	ELF1_LA07n	
A10	P31_IO+	ELF1_LA04p	
B10	P31_IO-	ELF1_LA04n	
C1	P31_IO+	ELF2_LA07p	
D1	P31_IO-	ELF2_LA07n	
C2	P31_IO+	ELF2_LA04p	
D2	P31_IO-	ELF2_LA04n	
C3	P31_IO+	ELF1_LA23p	
D3	P31_IO-	ELF1_LA22p	
C4	P31_IO+	ELF1_LA19p	
D4	P31_IO-	NC (+VADJ)[2]	No Connect or VADJ via Jumper
C5	P31_IO+	ELF1_LA16p	
D5	P31_IO-	NC (+VADJ)[2]	No Connect or VADJ via Jumper
C6	P31_IO+	ELF1_LA13p	
D6	P31_IO-	NC (+VADJ)[2]	No Connect or VADJ via Jumper
C7	P31_IO+	ELF1_LA11p	
D7	P31_IO-	ELF1_LA11n	
C8	P31_IO+	ELF1_LA09p	
D8	P31_IO-	ELF1_LA09n	
C9	P31_IO+	ELF1_LA06p	
D9	P31_IO-	ELF1_LA06n	
C10	P31_IO+	ELF1_LA03p	
D10	P31_IO-	ELF1_LA03n	
E1	P31_IO+	ELF2_LA06p	
F1	P31_IO-	ELF2_LA06n	
E2	P31_IO+	ELF2_LA03p	
F2	P31_IO-	ELF2_LA03n	
E3	P31_IO+	ELF1_LA21p	
F3	P31_IO-	NC	
E4	P31_IO+	ELF1_LA18_CCp	
F4	P31_IO-	NC	
E5	P31_IO+ / CC	ELF1_LA15p	
F5	P31_IO- / CC	NC	
E6	P31_IO+ / CC	ELF1_LA12p	
F6	P31_IO- / CC	NC	
E7	P31_IO+	ELF1_LA10p	
F7	P31_IO-	ELF1_LA10n	
E8	P31_IO+	ELF1_LA08p	
F8	P31_IO-	ELF1_LA08n	
E9	P31_IO+	ELF1_LA05p	
F9	P31_IO-	ELF1_LA05n	
E10	P31_IO+	ELF1_LA02p	
F10	P31_IO-	ELF1_LA02n	

[1] Polarity issue in version A.3 of the D1.0 specification,[See Section 3.2.1].
[2] Potential hole in the specification in that there could be an FPGA I/O voltage mismatch between the AMC board and the µRTM and ELF cards [See Section 3.2.2].

Table 2: J31 RTM Connector Pinout

4 Features

4.1 µRTM Management I²C Bus

ACQ400-MTCA-RTM-2 provides the standard management hardware as required by the MTCA.4 specification. These devices are all accessed via the standard I²C bus and are detailed as follows.

Provision has been made on the µRTM Management I²C bus to allow it to be combined with other µRTM management devices [See Section 4.2.1] via 0 Ω jumpers.

4.1.1 EEPROM

Device: M24C64
I²C Address: 0x50
A 64kbit (8Kbytes) EEPROM compatible with the MTCA.4 specification[1] is provided to store FRU and other information. The EEPROM may be write-protected to prevent accidental overwrites via the LED and Hot Swap Handle GPIO Expander [See Section 4.1.3].

4.1.2 Temperature Sensor

Device: LM75
I²C Address: 0x48
A temperature sensor compatible with IPMI v2.0 [See Section 0.2] as called for by the MTCA.4 specification is provided to monitor the temperature of the analogue power supplies.

4.1.3 LEDs and Hot Swap Handle GPIO Expander

Device: PCF8574A
I²C Address: 0x3E
An I²C GPIO expander is used for control and monitoring of the LEDs and Hot Swap handle respectively. A table of each pin and usage instructions is provided in Table 1. Each pin may be used as an input or an output without the use of a direction control register. Please see the datasheet for more information. This device and its connected I/Os matches the DESY reference design and is compatible with DESY MMC implementations.

Pin	Function	Dir	Active Low	Default	Usage[1]
P0	Handle Pulled	In	0	-	Low = Pushed Home High = Pulled
P1	Blue Hot Swap LED	Out	0	1 (PU)[2]	Low = Off High = On (Default)[3]
P2	Red LED (LED1)	Out	0	1 (PU)[2]	Low = Off High = On (Default)
P3	Green LED (LED2)	Out	1	0	Low = On High = Off (Default)
P4	NC	In			
P5	NC	In			
P6	NC	In			
P7	EEPROM Write Protect	Out	0	1 (PU)[2]	Low = Unprotected High = Protected (Default)

[1] Usage descriptions “High” and “Low” refer to actual output voltage levels.
[2] Pull-Up (PU) Resistor sets power-up default.
[3] REQ 3-15

Table 3: LED and Hot Swap Handle Management GPIO Expander

[1]REQ 3-8, 3-9 and 3-10

4.1.4 Unique ID

Device: 24AA025E48
I²C Address: 0x51
Provides a unique identifier for each board. This matches the DESY reference design.

4.2 FPGA I²C Bus

The ELF sites and other management functions are separated from the main I²C bus to prevent any possible address conflicts. The devices are connected through an I²C bus splitter to further mitigate potential address conflicts. The splitter and devices are described below.

See Figure 3 for an overview of how the I²C devices are connected.

If a dedicated I²C bus is not coming directly from the FPGA, D-TACQ recommends connecting the I²C lines via resistor jumpers to allow a carrier to be fully DESY D1.0 compliant.

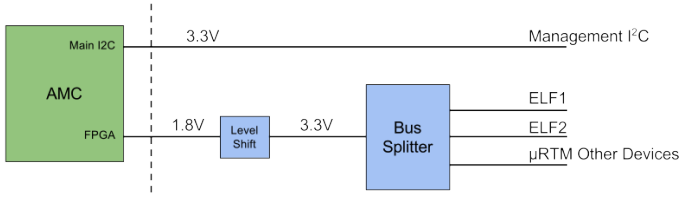


Figure 3: AMC- µRTM I²C Diagram

4.2.1 FPGA I²C Bus Splitter

Device: PCA9546A
I²C Address: 0x73
The bus splitter has three arms which should be selected individually. If one of the arms should hang, a dedicated reset line is provided from the Zone 3 connector. The reset line is active low and has a pullup to µRTM-MP.

Splitter Arm 0

The µRTM ELF Management I²C bus may be combined with other µRTM management devices via 0 Ω jumpers.

ELF Management GPIO

Device: Device: PCA9534
I²C Address: 0x21
An I²C GPIO expander is used for monitoring and reporting the status of the ELF sites as well as allowing control of the on-board ELF power supplies. A table of each pin, its configuration settings and usage instructions is provided in Table 4.

Please note the ELF LEDs are powered from the +12V µRTM-PWR rail to keep power consumption on the µRTM-MP Management Power rail within specification.

Typical bringup sequence of ELF modules is as follows:

1. Check Present lines.
2. If cards are present, inspect their EEPROMs for valid FRU files.
3. If FRUs are invalid or an appropriate FPGA bitstream is not available, set LEDs red (the +12V µRTM-PWR needs enabled by the AMC board to power the LEDs) whilst keeping the analogue and digital supplies disabled.

4. If FRUs are valid, and an appropriate FPGA bitstream is available, set LEDs green as appropriate, enable the analogue and digital power supplies (no sequencing is required for these), and load the appropriate bitstream.

If the FPGA I/O voltage is provided to the µRTM via the AMC, this should be gated by the AMC in a similar way to µRTM-PWR (+12V) and µRTM-MP (+3.3V) and enabled at the same time as the digital supplies.

Pin	Function	Dir	Active Low	Default	Usage[1]
P0	ELF1 Green LED	Out	0	0	Low = Off (Default) High = On
P1	ELF1 Red LED	Out	0	0	Low = Off (Default) High = On
P2	ELF2 Green LED	Out	0	0	Low = Off (Default) High = On
P3	ELF2 Red LED	Out	0	0	Low = Off (Default) High = On
P4	ELF1 Present	In	1		Low = Present High = Not Present
P5	ELF2 Present	In	1		Low = Present High = Not Present
P6	Analogue Supplies Enable	Out	1	0	Low = Enable High = Disable (Default)
P7	Digital Supplies Enable	Out	0	0	Low = Disable (Default) High = Enable

[1] Usage descriptions “High” and “Low” refer to actual output voltage levels.

Table 4: ELF Management GPIO

ELF Power Supply Monitor 1

Device: AD7417
I²C Address: 0x28
Two devices are provided for monitoring the levels of the on-board power supplies. Each supply is divided down to an appropriate level to be monitored by the device so equations to convert the input in Volts back to the actual rail voltage are given in Table 5. The negative voltage rail uses the +3.3V rail as a reference, therefore the +3.3V rail on ELF Power Supply Monitor 2 should be measured first.

The AD7417 also provides another temperature reading for the board.

Input	Voltage Rail	Input Conversion
1	$-V_{analogue}$	((input_in_V * 33) – (measured_3.3V_rail_in_V * 28)) / 5
2	$+V_{analogue}$	input_in_V * 11
3	$+5V_{analogue}$	input_in_V * 4.012
4	$+2.5V_{ref}$	input_in_V * 2

Table 5: ELF Power Supply Monitor 1 Inputs

ELF Power Supply Monitor 2

Device: AD7417
I²C Address: 0x29
Two devices are provided for monitoring the levels of the on-board power supplies. Each supply is divided down to an appropriate level to be monitored by the device so equations to convert the input in Volts back to the actual rail voltage are given in Table 6. Use the +3.3V input value as a reference for the -Vanalogue measurement on ELF Power Supply Monitor 1.

The AD7417 also provides another temperature reading for the board.

Input	Voltage Rail	Input Conversion
1	+2.5V	input_in_V * 2
2	+3.3V	input_in_V * 2
3	+1.8V	input_in_V * 2
4	+5Vref	input_in_V * 4.012

Table 6: ELF Power Supply Monitor 2 Inputs

4.2.2 Splitter Arm 1: ELF1

Note:
Early versions of the ACQ400-MTCA-RTM-2 used the FMC concept of "Geographical Addressing" for the I^2C devices on the ELF cards. This was different to standard D-TACQ practice on carrier cards which use "Non-Geographical Addressing" and was therefore changed to the D-TACQ standard "Non-Geographical Addressing".

This affects the addresses of the I2C devices on the ELF sites and hence operating system device tree calculation on where to find devices that each ELF board that may be fitted. Please contact info@d-tacq.com if there are any discrepancies between expected and actual addresses of these devices

Each ELF module provides a FRU EEPROM holding card identifying information. Each ELF module also typically provides an AD7417 to monitor temperature and voltage rails.

For example the standard AD7417 device (if present) and EEPROM will have addresses as given below.

EEPROM

Device: M24C64
I^2C Address: 0x50
This contains FRU information such as card model, serial number, etc.

Power Supply Monitor

Device: AD7417
I^2C Address: 0x28
The monitored voltages on these devices typically vary between modules due to their different supply requirements. Please contact info@d-tacq.com for details of voltages and conversion equations for specific modules.

Other Devices

Some cards also have GPIO expanders providing extra functionality to a board such as gain control. Please contact info@d-tacq.com for individual module requirements.

4.2.3 Splitter Arm 2: ELF2

This bus is the same as Splitter Arm 1 ELF1, Section 4.2.2 above

4.3 Front-Panel Clock

A Single Pin LEMO 00 Series Mini Coax connector (part EPL.00.250.NTN) is provided on the µRTM faceplate allowing an external signal to be applied as a sample clock for any ELF modules.
Mating plugs should be compatible with this part
The Pinout is Input on the Centre Pin and 0V on the shield.
Input voltage range of the connector is standard TTL: 0 to +5V.

The incoming clock signal is converted to an LVDS differential pair (matching the DESY D1.0 specification) and output on the Zone 3 connectors.
The LVDS receiver is an Onsemi NB6N11S
Due to the input containing an over-voltage clamp diode, the external clock input is only available if the digital supplies are enabled.

Usage of this clock signal is dependent on the AMC board that the RTM is connected too.

4.4 Voltage Rails

Each ELF module has different voltage and power requirements. The supplies on-board ACQ400-MTCA-RTM-2 provide enough power for every combination of module. No two ELF cards will require a current draw from the AMC module of more than 2A, as defined by the MTCA.4 specification[2]. Depending on the configuration, typical power usage will be much lower.

Contact info@d-tacq.com for typical power requirements of individual cards.

4.5 Digital Power Supplies

On-board digital supplies are +1.8V, +2.5V, +3.3V and +5$V_{analogue}$. The ELF modules will never use all of the available current – the overhead is present to allow for the requirements of all of the different modules. These are software controlled and monitored via I^2C [See Table 5 and Table 6].

[2] REQ 4-11

4.6 Analogue Power Supplies

On-board power supplies provide clean analogue power rails to the ELF modules. Factory-fitted sitchable options are ±13V or ±7V. Depending on the application and the desired input or output voltage range of the ELF modules, these values are selected power usage may be reduced by setting SW2 [See Figure 4] to HI or LO as appropriate.

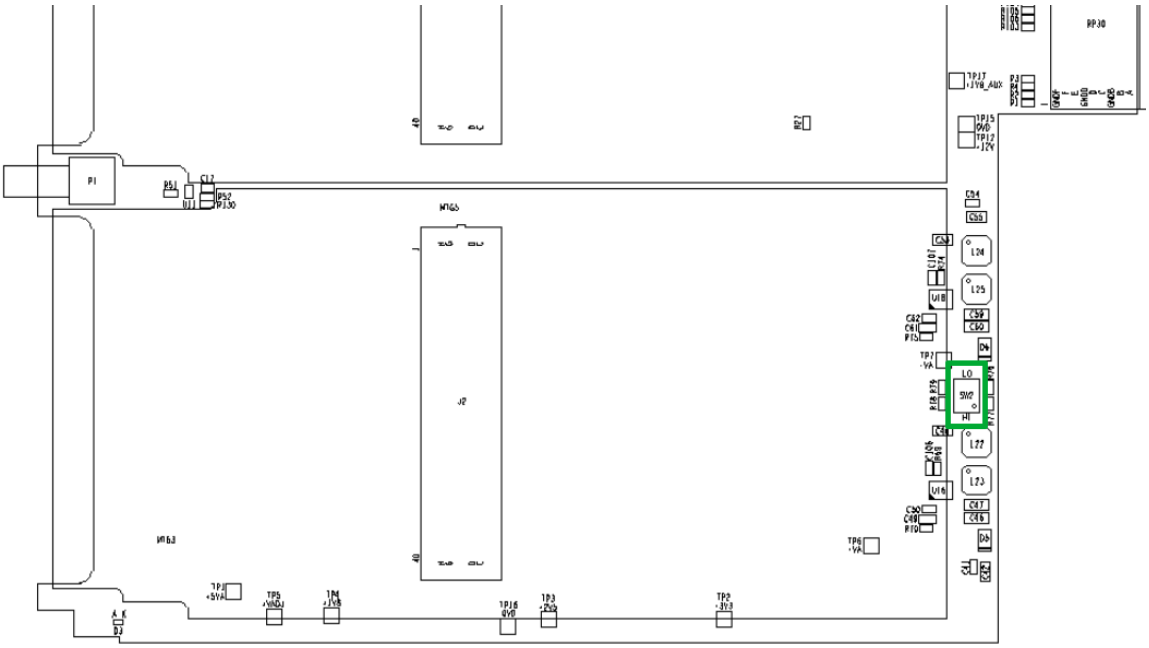


Figure 4: Location of Analogue Power Switch

The analogue power supplies are enabled [See Table 4] and monitored [See Table 5] over I^2C.

SW2 Setting	Analogue Supply Voltages	Typical I/O Voltage Range
HI	±13V	±10V
LO	±7V	±5V

Table 7: Analogue Voltage Power Switch Settings

4.7 Analogue Voltage References

On-board voltage reference chips provide highly accurate $+2.5V_{ref}$ and $+5V_{ref}$ reference voltages for the ELF modules' ADCs and DACs. These are powered from the positive analogue voltage rail and are therefore enabled with the analogue supplies [See Table 4]. The voltage references can also be monitored over I^2C [See Table 5 and Table 6].

5 Electrical Specification

Parameter	Min	Typ	Max	Unit	Notes
µRTM-MP[1]Voltage		3.3		V	
µRTM-MP Current			30	mA	
µRTM-PWR Voltage		12		V	
µRTM-PWR Current		1.5	2.5	A	Assuming 10W and 15W per ELF site for Typ and Max respectively.[2]
I^2C, JTAG Voltage		3.3		V	
FPGA I/O Voltage		1.8 - 3.3		V	Zone 3 connectors are currently fully compliant with D1.0 spec, however we would recommend generating the I/O voltage on the front AMC card and using some spare pins to provide this power and avoid any potential mismatches.
FPGA I/O Current			300	mA	Maximum required current for an AMC-side +1.8V supply for ELF module I/O if implemented.

[1] MP: Management Power
[2] Power usage varies depending on the fitted ELF modules. Please contact info@d-tacq.com for more details.

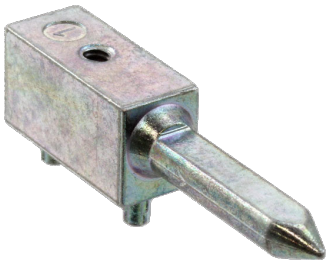
Table 8: Electrical Specification

6 ACQ400-MTCA-RTM-2 MTCA and D1.0 Specification

Parameter	Notes
Module Type	Double-width, Mid-size
Zone 3 Connectors	2x 30-pair TE Connectivity 6469183-1
Mechanical Keying	DN = 1; A = 0°; TE Connectivity 1469265-1

Table 9: ACQ400-MTCA-RTM-2 Specification

The mechanical keying is shown in the picture below



The Standard FRU information for the RTM will be similar to the report below

```
ipmitool -H mtca-crate3 -v -P "" -B 0 -b 7 -T 0x82 -t 0x76 fru print 1
Running Get PICMG Properties my_addr 0x20, transit 0, target 0x20
Discovered PICMG Extension Version 5.0
Discovered IPMB address 0x20
Discovered Target IPMB-0 address 0xff
Board Mfg Date        : Fri Mar 22 09:00:00 2024
Board Mfg             : D-TACQ Solutions
Board Product         : ACQ400-MTCA-RTM-2
Board Serial          : CM4020118
Board Part Number     : ACQ400-MTCA-RTM-2-NG
Product Manufacturer  : D-TACQ Solutions
Product Name          : ACQ400-MTCA-RTM-2
Product Part Number   : ACQ400-MTCA-RTM-2-NG
Product Version       : B04
Product Serial        : CM4020118
PICMG Extension Record
FRU_AMC_CURRENT
Current draw(@12V): 2.00 A [ 24.00 Watt ]

PICMG Extension Record
Unknown OEM Extension Record ID: 30
```

Revision History

Revision	Date	Author(s)	Description
1	09/09/2024	JMcL	Created