ACQ427ELF
Product Specification

High Performance Simultaneous Data Acquisition

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1 Product Description

1. ***ACQ427ELF*** is a 8 channel simultaneous Analog Input module, with 4 simultaneous Analog Outputs.
2. Standard configuration :

   ACQ427ELF-03-10000-16:

   1. 8 AI channels, 1000kSPS/16 bit,
   2. 4 AO channels, 1000kSPS/16 bit.

   ACQ427ELF-02-1000-16

   1. 4 AI channels, 1000kSPS/16bit.
   2. 4 AO channels, 1000kSPS/16bit

   ACQ427ELF-01-1000-16

   1. 8 AI channels, 1000kSPS/16 bit.
   2. 0 AO channels.
3. Extended module with *FMC* connector and *FMC* front panel.
4. 2-wire Differential inputs, high quality instrument amplifier front end with switched input voltage ranges.
5. Front panel connector: 4 x Single Pin Lemo, SPL floating shell.
6. Additional channel connectors: 4 x SPL, floating shell, “TOPDECK”

1.1 Product Variants

- ***ACQ427ELF-0[123]-1000-16*** : AI: 1000kSPS/channel, 16 bit
- ***ACQ427ELF-0[123]-2000-16*** : AI: 2000kSPS/channel, 16 bit
- ***ACQ427ELF-0[123]-1000-18*** : AI: 1000kSPS/channel, 18 bit

In all cases, AO is specified as 16 bit, 1000kSPS.

1.2 Applications

- Instrumentation applications, control and monitoring.

1.3 Overview

The *ELF* module standard adds user IO to carrier modules fitted with *FPGA* resource. D-TACQ recommends modules based on the *Xilinx ZYNQ* system on chip, combining *FPGA* resource with a dual-core ARM Cortex A9 and gigabit Ethernet. Compatible modules include

- D-TACQ ***ACQ1001*** : D-TACQ single slot *FMC* carrier, Z7020, up to 12 SPL
- D-TACQ ***ACQ2106*** : D-TACQ 6 site *ELF* carrier, Z7030 : 8 SPL per site.
- KMCUZ30: Micro TCA, 2 site ELF carrier, Z7030: 4 SPL per site
- PandA : 1U x 19” box, Z7030, single TOPDECK: 8 SPL

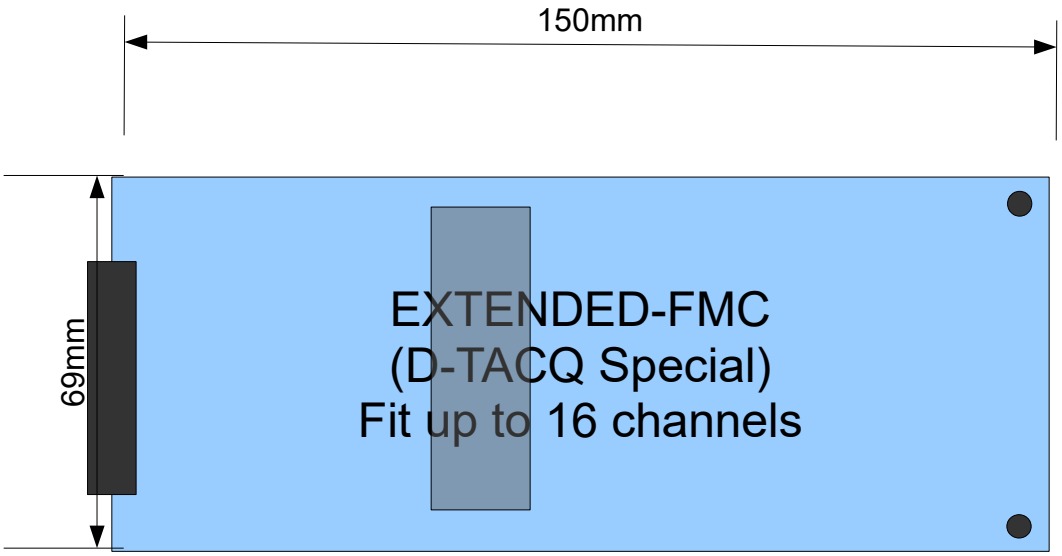
D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

1.4 Glossary

- *FMC*: VITA57 FPGA Mezzanine Card.
- Xilinx ZYNQ System-on-chip.
- *LPC* : *FMC* Low pin count wiring standard.
- *ULPC*: *FMC* Ultra low pin count (D-TACQ).
- Extended, E : *FMC* Extended size module (D-TACQ).

2 Physical

Extended FMC Module



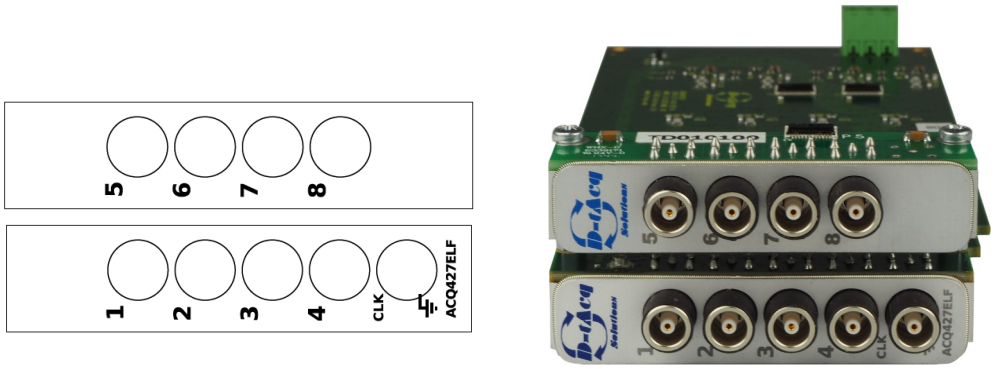
2.1 Example 1: Fitted to ACQ1001 Carrier

Carrier fits 1 x standard FMC eg ***ACQ420FMC*** or or an extended size module eg ***ACQ427ELF***

2.2 Appearance

2.2.1 Standard Front Panel

The standard front panel setup is shown and is an 8 Analog Input Configuration as shown below



Channels 1-4 are on the bottom row and channels 5-8 on the top row on the TOPDECK with channel numbers ascending left to right.

The bottom right connection is for an input sample clock.

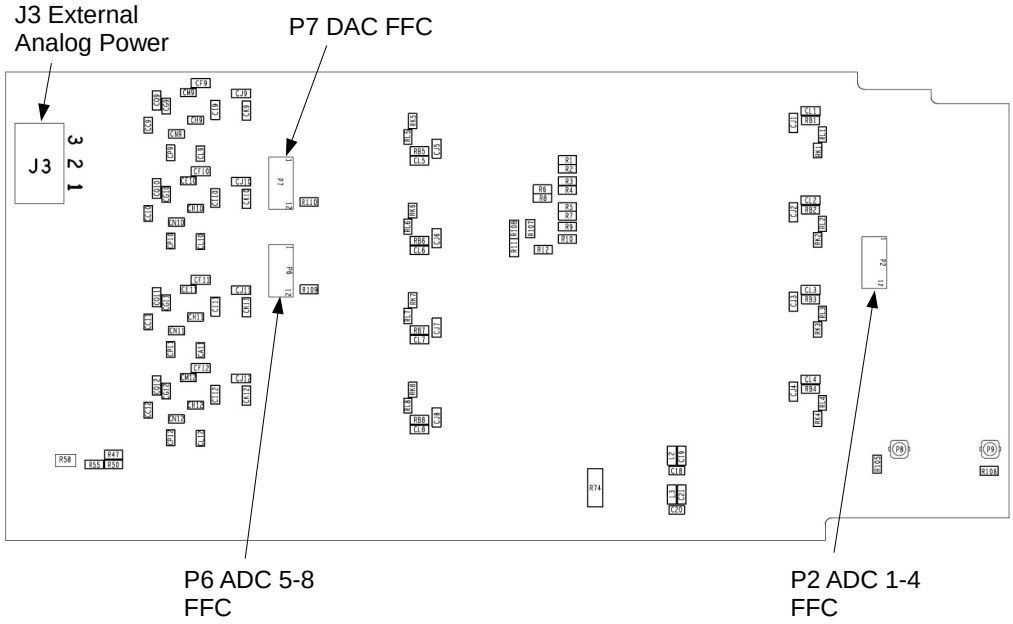
2.2.2 Optional Front Panels

The Front Panel configuration can vary according to the channel connections regarding number of Analog Input channels and the number of Analog Output channels.
Please contact D-TACQ for details

Example below shows a custom Dual-Pin LEMO Front Panel Configuration

2.2.3 Internal Connections

The ACQ427ELF is normally supplied fully configured however for use on third party carrier boards and when the top row connections are to be reassigned this requires the following connections



J3 External Analog Power Connector

Pin Number	***Description***
1	+15V Analog Power
2	0V
3	-15V Analog Power

The FFC cables are connected as follows

Configuration	***FFC Connections***
8 Analog Inputs (8AI)	TOPDECK to P6
4 Analog Inputs (4AI) 4 Analog Outputs (4AO)[1]	TOPDECK to P7
4 Analog Inputs (4AI) Double Sampled[2]	No TOPDECK FFC between P2 and P6

1 If the 4AI and 4AO configuration is made on a board with an 8AI Front Panel then channels 5-8 on the Front Panel are Analog Out 1-4.

2 Please Contact D-TACQ, this mode connects channels 5-8 to the 1-4 inputs to allow the sampling of each channel by 2 ADCs to increase resolution.

3 ACQ427ELF AI Electrical Specification.

#	Parameter	Value
1	Number of Channels	8
2	Sample Rate	up to 2000 kHz, per channel simultaneous
3	Resolution	16 [18] bits
4	Coupling	DC, Differential Input
5	Input Impedance	1 MΩ
6	 Input Voltage Range Standard (1,2,4,8) High Gain (1,10,100,1000)	Software selectable ranges. ±10V,±5V,±2.5V,±1.25V ±10V,±1V,±100mV,±10mV
7	Input Voltage Withstand	±30V
8	Offset Error	0.01% FS with numerical calibration
9	Gain Error	0.01% FS with numerical calibration
10	INL	16 bit ±0.2 LSB 18 bit ±0.5 LSB
11	DNL	16 bit ±0.1 LSB 18 bit ±0.1 LSB
12	CMRR	>80dB FS @ 1 kHz
13	THD	-95 dB*
14	SINAD	-88 dB*
15	SFDR	100 dBc*
16	SNR Gain *1 SNR Gain *2 SNR Gain *4 SNR Gain *8	94 dB* subject to final qualification 94 dB* subject to final qualification 92 dB* subject to final qualification 90 dB* subject to final qualification
17	Power BW (-3 dB)**	450 kHz
18	Small Signal BW**	-1000: 500 kHz -2000: 800 kHz
19	Crosstalk	<90 dB @ 1 kHz FS Input
20	Temperature Stability	<25 ppm/C

Typical values

* Typical values measured at full scale with a 9.76kHz input
** Bandwidth is reduced in High Gain configuration. Contact factory for details

4 ACQ427ELF AO Electrical Specification

#	Parameter	Value
1	Number of Channels	4
2	Sample Rate	Up to 1000 kHz, per channel simultaneous
3	Resolution	16 bits
4	Coupling	DC, Single-ended Output
5	Maximum output current	20 mA per channel
6	Output Voltage Range	±10 V ±5V
7	Output Impedance	33Ω
8	Offset Error	0.01% FS with numerical calibration
9	Gain Error	0.01% FS with numerical calibration
10	INL	±2 LSB
11	DNL	±1 LSB
12	THD	92 dB
13	SINAD	89 dBc
14	SFDR	95 dBc
15	SNR	90 dB
16	Full Power BW	50kHz Standard [250kHz, 5kHz Options]
17	Crosstalk	<95 dB @ 1 kHz FS
18	Temperature Stability	<25 ppm/C

5 ACQ427 FMC Connector Pinout

FMC Pin	Function
p_FMC_CLK0_M2C_n	Not Used
p_FMC_CLK0_M2C_p	DAC_SCK
p_FMC_CLK1_C2M_n	Not used
p_FMC_CLK1_C2M_p	Not used
p_FMC_LA00_CC_n	Not used
p_FMC_LA00_CC_p	EXT_CLK
p_FMC_LA01_CC_n	Not used
p_FMC_LA01_CC_p	DAC_SYNC_n
p_FMC_LA02_n	Not used
p_FMC_LA02_p	DAC_LOAD_n
p_FMC_LA03_n	Not used
p_FMC_LA03_p	DAC_RESET_n
p_FMC_LA04_n	Not used
p_FMC_LA04_p	DAC CH01 SDI (DAC_4_SDI)
p_FMC_LA05_n	Not used
p_FMC_LA05_p	DAC CH02 SDI (DAC_3_SDI)
p_FMC_LA06_n	Not used
p_FMC_LA06_p	DAC CH03 SDI (DAC_2_SDI)
p_FMC_LA07_n	Not used
p_FMC_LA07_p	DAC CH04 SDI (DAC_1_SDI)
p_FMC_LA08_n	Not used
p_FMC_LA08_p	DAC CH01 SDO (DAC_4_SDO)
p_FMC_LA09_n	Not used
p_FMC_LA09_p	DAC CH02 SDO (DAC_3_SDO)
p_FMC_LA10_n	Not used
p_FMC_LA10_p	DAC CH03 SDO (DAC_2_SDO)
p_FMC_LA11_n	Not used
p_FMC_LA11_p	DAC CH04 SDO (DAC_1_SDO)
p_FMC_LA12_n	Not used
p_FMC_LA12_p	EXT_TRIG
p_FMC_LA13_n	Not used
p_FMC_LA13_p	ADC_SCK
p_FMC_LA14_n	Not used
p_FMC_LA14_p	ADC_CNV_A
p_FMC_LA15_n	Not used
p_FMC_LA15_p	ADC_CNV_B
p_FMC_LA16_n	Not used
p_FMC_LA16_p	ADC CH01 SDO (ADC_A4_SDO)
p_FMC_LA17_CC_n	Not used
p_FMC_LA17_CC_p	ADC CH02 SDO (ADC_A3_SDO)
p_FMC_LA18_CC_n	Not used
p_FMC_LA18_CC_p	ADC CH03 SDO (ADC_A2_SDO)
p_FMC_LA19_n	Not used
p_FMC_LA19_p	ADC CH04 SDO (ADC_A1_SDO)
p_FMC_LA20_n	Not used
p_FMC_LA20_p	ADC CH05 SDO (ADC_B4_SDO)

p_FMC_LA21_n	Not used
p_FMC_LA21_p	ADC CH06 SDO (ADC_B3_SDO)
p_FMC_LA22_n	Not used
p_FMC_LA22_p	ADC CH07 SDO (ADC_B2_SDO)
p_FMC_LA23_n	Not used
p_FMC_LA23_p	ADC CH08 SDO (ADC_B1_SDO)

6 I2C Expander Connections

I2C Expander Port	Schematic Net	Function
P00	ADC_A1_A0	CH04 Gain Select LSB
P01	ADC_A1_A1	CH04 Gain Select MSB
P02	ADC_A2_A0	CH03 Gain Select LSB
P03	ADC_A2_A1	CH03 Gain Select MSB
P04	ADC_A3_A0	CH02 Gain Select LSB
P05	ADC_A3_A1	CH02 Gain Select MSB
P06	ADC_A4_A0	CH01 Gain Select LSB
P07	ADC_A4_A1	CH01 Gain Select MSB
P08		
P09		
P10	ADC_B1_A0	CH08 Gain Select LSB
P11	ADC_B1_A1	CH08 Gain Select MSB
P12	ADC_B2_A0	CH07 Gain Select LSB
P13	ADC_B2_A1	CH07 Gain Select MSB
P14	ADC_B3_A0	CH06 Gain Select LSB
P15	ADC_B3_A1	CH06 Gain Select MSB
P16	ADC_B4_A0	CH05 Gain Select LSB
P17	ADC_B4_A1	CH05 Gain Select MSB
P18		
P19		
P20	CLK_DIR	Clock Direction
P21	TRIG_DIR	Trigger Direction
P22	DAC_RIBBON	DAC Ribbon Detect (Connector P7)
P23	ADC_B_RIBBON	ADC_B Ribbon Detect (Connector P6)
P24	DAC_3_RANGE	DAC_2_RANGE
P25	DAC_4_RANGE	DAC_1_RANGE
P26	DAC_1_RANGE	DAC_4_RANGE
P27	DAC_2_RANGE	DAC_3_RANGE

7 Gain Selection

A1 (MSB) Line from I2C Expander	A0 (LSB) Line from I2C Expander	Selected Gain
LOW	LOW	1 (+/-10V)
LOW	HIGH	2 (+/-5V)
HIGH	LOW	4 (+/-2.5V)
HIGH	HIGH	8 (+/-1.25V)