Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I^2C, optional JTAG support

Digital signals in the user zone:
- Class D1.0: 48 LVDS I/O signals
- Class D1.1: 42 LVDS I/O signals, 2 high-speed links
- Class D1.2: 38 LVDS I/O signals, 4 high-speed links
- Class D1.3: 28 LVDS I/O signals, 8 high-speed links
- Class D1.4: 8 LVDS I/O signals, 16 high-speed links

Digital signals with a fixed direction:
- 2 LVDS low phase noise clocks
- 1 LVDS timing output signal
- 3 LVDS outputs for user applications

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- High-speed data processing
- Multi-channel data-converters, sensor readout and output
- Digital signal conditioning boards

GENERAL DESCRIPTION

This Class D1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring digital signals over the Zone 3 connector. This digital class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The subclasses offers different numbers of digital input / outputs and high-speed communication links. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

This Class D1.x pin assignment requires a common µRTM management implementation to make AMC and µRTM boards compatible. Appropriate management interface templates for this Class are available on http://mtca.desy.de.

ZONE DESCRIPTION

The management zone (J30 row 1-2) is reserved for the µRTM management in the MTCA.4 standard. The pin assignment of class D1.0 offers 48 LVDS input / output signals. To achieve a high compatibility between AMC and µRTM boards, all used input and output signals (P30_IO, P31_IO) have to be programmable in direction and signal type, preferable by an FPGA located on the AMC side. The other classes offers 42, 38, 28 or 8 general purpose LVDS inputs / outputs. Depending on the class, 0, 2, 4, 8 or 16 high-speed serial communication interfaces (GTPx_Rx, GTPx_Tx) with clock signals (GTPx_CLK_IN, GTPx_CLK_OUT) for both directions are provided. Two digital LVDS clocks (J30 3ab,3cd), 3 general purpose LVDS outputs (J30 4cd,4ef,3ef) and a timing signal AMC_TCLK to the µRTM are available. These signals are driven from standard LVDS devices with fixed signal direction.

SEQUENCE OF SIGNAL OCCUPATION AND FPGA CLOCK REGIONS

To achieve a high compatibility between AMC and µRTM boards one should use a common sequence for the signal occupation:

Digital LVDS outputs:	(J30 4cd), (J30 4ef), (J30 3ef)
Digital LVDS inputs / outputs:	(J30 5ab), (J30 5cd), (J30 5ef), (J30 6ab), …, (J31 10ef)
Digital high-speed links with clocks:	(J31 row 10), (J31 row 9), … , (J30 row 5)
Primary clock capable pins “CC*”:	(J30 5ab), (J30 6ab), (J30 9ab), (J30 10ab), (J31 7ab), (J31 8ab) occupy first
Secondary clock capable pins “CC” :	(J30 7ef), (J30 8ef), (J31 3ab), (J31 4ab), (J31 5ef), (J31 6ef)

CC-Pins / FPGA Zones			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
1st FPGA Bank		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
		5	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
2nd FPGA Bank		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+ / CC	P31_IO+ / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+ / CC	P31_IO+ / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
3rd FPGA Bank		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		7	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		9	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		10	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-

Table 1 : FPGA clock regions and clock capable pins marked as “CC” for Class D1.0, D1.1, D1.2, D1.3, D1.4, AMC side view

Table 2,3 and 4 summaries the pin assignment, electrical specification and quiescent signal condition for the Class D1.0. The signal (AMC_CLK1+,AMC_CLK1-) provides typically a clock from the AMC to the µRTM and (RTM_CLK1+,RTM_CLK1-) vice versa. The (AMC_TCLK+, AMC_TCLK-) signal offers a long-term stable timing signal, splitted from the TCLKA signal, to provide e.g. RESET signals to clock sections on the µRTM. The LVDS output signals OUT0, OUT1, OUT2 can be used for general purpose. To avoid electric shorts during the insertion and extraction process of the µRTM all outputs with fixed direction of the zone (J30 row 3-4) have to be disabled via buffers on the AMC side controlled by the Module Management Controller (MMC).

AMC ZONE 3 PIN ASSIGNMENT RECOMMENDATION for Class D1.0

Class D1.0 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User -configuration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		7	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		9	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		10	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-

Table 2 : Pin assignment of Class D1.0, AMC side view

ELECTRICAL SPECIFICATION for Class D1.0

Clas D1.0 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	LVDS - O	LVDS - O	LVDS - I	LVDS - I	LVDS - O	LVDS - O
		4	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O
User -configuration		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		9	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		10	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
User -configuration	J31	1	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		2	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		3	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		9	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		10	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O

Table 3 : Electrical specification of Class D1.0 ("I"=input (µRTM to AMC), "O"=output (AMC to µRTM)), AMC side view

QUIESCENT SIGNAL CONDITIONS for Class D1.0

Class D1.0 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
Digital clocks fixed I/O		3	Disabling via Buffer	Disabling via Buffer			Disabling via Buffer	Disabling via Buffer
		4	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer
User -configuration		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		6	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		7	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		8	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		9	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		10	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
User Configuaration	J31	1	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		2	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		3	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		4	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		6	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		7	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		8	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
Standard Gbit-Links		9	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		10	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA

Table 4 : Quiescent signal conditions for Class D1.0, AMC side view

AMC ZONE 3 PIN ASSIGNMENT RECOMMENDATION for Class D1.1, D1.2, D1.3, D1.4

Class D1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		7	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
Standard Gbit-Links		9	GTP0-1_CLK_IN+	GTP0-1_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-1_CLK_OUT+	GTP0-1_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

Class D1.2 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
Standard Gbit-Links		7	P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

Class D1.3 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
Standard Gbit-Links		3	P31_IO+ / CC	P31_IO- / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
		4	P31_IO+ / CC	P31_IO- / CC	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5	GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6	GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7	P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

Class D1.4 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Standard Gbit-Links		5	P30_IO+ / CC *	P30_IO+ / CC *	GTP15_RX+	GTP15_RX-	GTP15_TX+	GTP15_TX-
		6	P30_IO+ / CC *	P30_IO+ / CC *	GTP14_RX+	GTP14_RX-	GTP14_TX+	GTP14_TX-
		7	GTP12-15_CLK_IN+	GTP12-15_CLK_IN-	GTP13_RX+	GTP13_RX-	GTP13_TX+	GTP13_TX-
		8	GTP12-15_CLK_OUT+	GTP12-15_CLK_OUT-	GTP12_RX+	GTP12_RX-	GTP12_TX+	GTP12_TX-
		9	P30_IO+ / CC*	P30_IO+ / CC*	GTP11_RX+	GTP11_RX-	GTP11_TX+	GTP11_TX-
		10	P30_IO+ / CC*	P30_IO+ / CC*	GTP10_RX+	GTP10_RX-	GTP10_TX+	GTP10_TX-
Standard Gbit-Links	J31	1	GTP8-11_CLK_IN+	GTP8-11_CLK_IN-	GTP9_RX+	GTP9_RX-	GTP9_TX+	GTP9_TX-
		2	GTP8-11_CLK_OUT+	GTP8-11_CLK_OUT-	GTP8_RX+	GTP8_RX-	GTP8_TX+	GTP8_TX-
		3	P31_IO+ / CC	P31_IO- / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
		4	P31_IO+ / CC	P31_IO- / CC	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5	GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6	GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7	P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

Table 5 : Pin assignment of Class D1.1, D1.2, D1.3, D1.4, AMC side view

ELECTRICAL SPECIFICATION for Class D1.1, D1.2, D1.3, D1.4

Class D1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	LVDS - O	LVDS - O	LVDS - I	LVDS - I	LVDS - O	LVDS - O
		4	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O
User -configuration		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		9	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		10	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
User Configuaration	J31	1	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		2	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		3	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
Standard Gbit-Links		9	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		10	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O

Class D1.2 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	LVDS - O	LVDS - O	LVDS - I	LVDS - I	LVDS - O	LVDS - O
		4	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O
User -configuration		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		9	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		10	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
User Configuaration	J31	1	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		2	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		3	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
Standard Gbit-Links		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		9	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		10	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O

Class D1.3 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	LVDS - O	LVDS - O	LVDS - I	LVDS - I	LVDS - O	LVDS - O
		4	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O
User -configuration		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		9	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		10	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
User Configuaration	J31	1	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		2	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
Standard Gbit-Links		3	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		5	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		6	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		9	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		10	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O

Class D1.4 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	LVDS - O	LVDS - O	LVDS - I	LVDS - I	LVDS - O	LVDS - O
		4	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O	LVDS - O
Standard Gbit-Links		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		6	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		7	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		8	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O
		9	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		10	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
Standard Gbit-Links	J31	1	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		2	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O
		3	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		5	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		6	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O
		7	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		8	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	CML - I	CML - I	CML - O	CML - O
		9	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
		10	LVDS - O	LVDS - O	CML - I	CML - I	CML - O	CML - O

Table 6 : Electrical specification of Class D1.x (“I”=input (µRTM to AMC), “O”=output (AMC to µRTM)), AMC side view

ELECTRICAL SPECIFICATION

The electrical specification of Zone 3 for the Classes D1.x are given in Table 3, 6. All input and output signals (P30_IO, P31_IO) of the user zone can be LVDS, LVCMOS or open collector (OC) typically provided by an FPGA. LVCMOS or OC outputs needs on the µRTM a power supply voltage adjustment mechanism provided by the management. Using I^2C communication OC signals in the user zone are assumed to be terminated on the µRTM side. To reduce the electromagnetic interference in the crate differential signals are recommended. High speed communication links having LVDS signals for clocks and CML levels on the receiver and transmitter side. Primary clock capable pins are marked as "CC*", secondary as "CC". Clocks for synchronizing high-speed interfaces are available in both directions. This allows placing synchronization circuits onto the AMC or µRTM board. Special configuration lines for the appropriate high-speed interfaces can be placed in J31 7ab, 8ab for GTP0-3, J31 3ab, 4ab for GTP4-7, J30 9ab, 10ab for GTP8-11 or J30 5ab, 6ab for GTP12-15. GTP transceivers should be AC-coupled on each transceiver side.

AMC MODULE AND µRTM PROTECTION

According to the PICMG MTCA.4 R1.0, section 3.5.7, ¶79 the insertion and extraction process of an µRTM needs an application specific quiesce action, e.g. no action, isolation of signals or power off the AMC controlled by the MMC. All AMC output signals with fixed direction of Class D1.x compatible modules have to be disabled via buffers on the AMC side controlled by the MMC. In addition these signals can be disabled or enabled application specific independent of the MMC protection mechanism.

Modern FPGAs offer a wide range of single- and differential ended input and output levels using different supply voltage banks. Here LVDS_25, LVCMOS_25, CML and open collector levels at 2.5V in the user zone are interesting. FPGA signals can be isolated during the insertion process, other devices rather not. Most of the devices have protecting diodes for the inputs and outputs mainly only against short transient currents, as depicted in Fig.1. In case of an unpowered µRTM, the active output stages of the AMC module will dissipate continuously power into the µRTM protection diodes. Depending on the output stage of Fig.2 the maximum short-to-GND currents are given by 40mA for LVDS_25, 50mA for CML, 200mA for LVCMOS_25 and approx. 2.5mA for OC_25 (open collector). According to Table 7 of the MTCA.4 standard, AMC and µRTM boards need a module hardware keying.

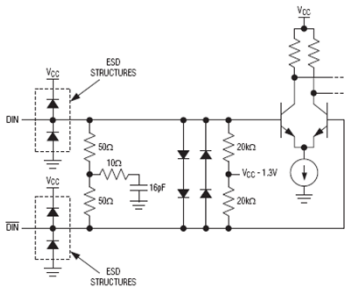
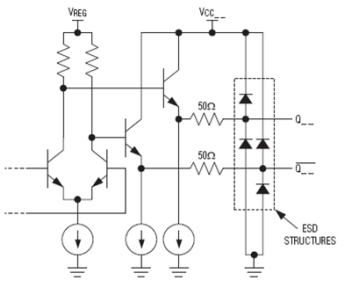
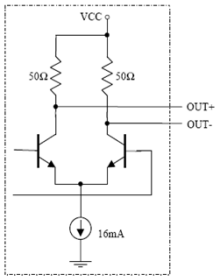


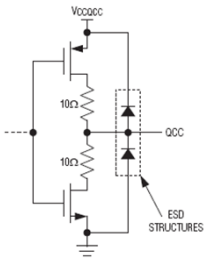
Fig.1 : Differential input stage

N	Data Signal in Volts
1	LVDS
2	0 – ±1
3	>±1 – ±3.3
4	>±3.3 – ±10
5	>±10
6	Reserved
7	Reserved
8	Reserved

Table 7: Mechanical module keying







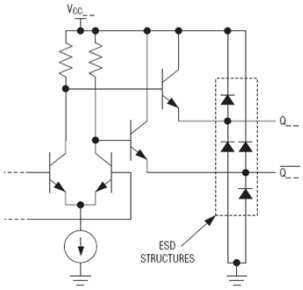


Fig.2: (a) LVDS output stage (b) CML output stage (c) LVCMOS output stage (d) LVPECL output stage

Table 4, 8 shows the AMC output signals, which have to be isolated, disabled or tri-stated on the AMC side in Class D1.x. The recommended protection method for the signals is listed. The FPGA gets the disabling information directly from MMC.

Idle state, AC-coupled	(GTPx_Tx+, GTPx_Tx-) state should be set to IDLE mode by FPGA on the AMC and µRTM. To remove common mode CML-levels, an AC-coupling has to be used on each transceiver side.
Disabling via FPGA	FPGA signals (P30_IO, P31_IO) can be disabled via FPGA itself from MMC.
Disabling via buffer	LDVS outputs with fixed signal direction have to be disabled by using a buffer with output enable. The disabling information is provided by the MMC. Depending on the application the buffer speed and jitter performance has to be considered. For AMC_TCLK a jitter of less than about 0.5ps is recommended.

QUIESCENT SIGNAL CONDITIONS for Class D1.1, D1.2, D1.3, D1.4

Class D1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
Digital clocks fixed I/O		3	Disabling via Buffer	Disabling via Buffer			Disabling via Buffer	Disabling via Buffer
		4	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer
User -configuration		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		6	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		7	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		8	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		9	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		10	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
User Configuaration	J31	1	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		2	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		3	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		4	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		6	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		7	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		8	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
Standard Gbit-Links		9			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		10	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled

Class D1.2 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
Digital clocks fixed I/O		3	Disabling via Buffer	Disabling via Buffer			Disabling via Buffer	Disabling via Buffer
		4	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer
User -configuration		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		6	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		7	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		8	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		9	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		10	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
User Configuaration	J31	1	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		2	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		3	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		4	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		6	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		7	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		8	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
Standard Gbit-Links		9			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		10	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled

Class D1.3 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
Digital clocks fixed I/O		3	Disabling via Buffer	Disabling via Buffer			Disabling via Buffer	Disabling via Buffer
		4	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer
User -configuration		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		6	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		7	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		8	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		9	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		10	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
User Configuaration	J31	1	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		2	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		3	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		4	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		5			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		6	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		7	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		8	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
Standard Gbit-Links		9			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		10	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled

Class D1.4 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
Digital clocks fixed I/O		3	Disabling via Buffer	Disabling via Buffer			Disabling via Buffer	Disabling via Buffer
		4	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer
User -configuration		5	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		6	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		7			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		8	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		9	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		10	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
User Configuaration	J31	1			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		2	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		3	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		4	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		5			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		6	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		7	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		8	Disabling via FPGA	Disabling via FPGA	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
Standard Gbit-Links		9			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
		10	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled

Table 8 : Quiescent signal conditions for Class D1.1, D1.2, D1.3, D1.4 , AMC side view

After inserting the µRTM a compatibility check of the Zone 3 has to performed according to the MTCA.4. After successful acceptance, the µRTM payload power can be switched on. If an µRTM is extracted via hot-swap handle, the µRTM has to be switched off via MMC and the AMC has to set the Zone 3 signals into the disabled state, as well after power cuts and failures. All µRTM output signals do not have to be isolated, because they are powered down during the insertion process. Isolating analog or low-jitter clock signals will degrade their performance and is no option in this class.

ZONE 3 TERMINATION AND SUBCLASS COMPATIBILITY

To achieve a high compatibility between the different digital subclasses FPGA pins and clock capable pins should be connected with the recommended filling sequence. GTP transceivers on the AMC and µRTM should be AC-coupled. To prevent an electrical LVDS to CML conflict, not supported GTPs from AMC or µRTM should be switched to the IDLE mode via management. AMCs should operate without µRTMs. If the AMC do not use the full functionality of the µRTM there should be no electrical conflict. Consequently input signals should be in general such terminated using pull-up/pull-down resistors on the receiver side, that a defined default electrical state is guaranteed and output signals should survive a missing termination.

The following items should be applied if the AMC or the µRTM does not support a signal function.

User configuration: The µRTM should let all unused signals open.
The AMC should let all unused signals open.

Digital fixed I/O: If the µRTM do not support the signal function, the µRTM should terminate signals of this group.
If AMC_TCLK, OUT0 , OUT1 or OUT2 is not used (implemented) by the AMC, it should let them open.
If the µRTM support the signal function it has to provide a default logic state for the signals OUT0, OUT1, OUT2.

GTP clock inputs: if a µRTM do not support a GTPx_CLK_IN signal it should be open on the µRTM side.
If an AMC do not support a GTPx_CLK_IN signal it should be terminated on the AMC side.

GTP clock outputs: If an AMC do not support a GTPx_CLK_OUT signal it should be open on the AMC side.
If a µRTM do not support a GTPx_CLK_OUT signal it should be terminated on the µRTM side.

Table 9, 10 shows the signal termination in Class D1.0 if the AMC, respectively µRTM does not support a signal function.

Class D1.0 / Zone			a	b	c	d	e	f
AMC Side								
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	open	open	differential terminated		open	open
		4	open	open	open	open	open	open
User -configuration		5	open	open	open	open	open	open
		6	open	open	open	open	open	open
		7	open	open	open	open	open	open
		8	open	open	open	open	open	open
		9	open	open	open	open	open	open
		10	open	open	open	open	open	open
User -configuration	J31	1	open	open	open	open	open	open
		2	open	open	open	open	open	open
		3	open	open	open	open	open	open
		4	open	open	open	open	open	open
		5	open	open	open	open	open	open
		6	open	open	open	open	open	open
		7	open	open	open	open	open	open
		8	open	open	open	open	open	open
		9	open	open	open	open	open	open
		10	open	open	open	open	open	open

Table 9: Signal termination in Class D1.0 if the AMC does not support a signal function, AMC side view

Class D1.0 / Zone			a	b	c	d	e	f
RTM Side								
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	differential terminated		open	open	differential terminated	
		4	differential terminated		differential terminated		differential terminated	
User -configuration		5	open	open	open	open	open	open
		6	open	open	open	open	open	open
		7	open	open	open	open	open	open
		8	open	open	open	open	open	open
		9	open	open	open	open	open	open
		10	open	open	open	open	open	open
User -configuration	J31	1	open	open	open	open	open	open
		2	open	open	open	open	open	open
		3	open	open	open	open	open	open
		4	open	open	open	open	open	open
		5	open	open	open	open	open	open
		6	open	open	open	open	open	open
		7	open	open	open	open	open	open
		8	open	open	open	open	open	open
		9	open	open	open	open	open	open
		10	open	open	open	open	open	open

Table 10: Signal termination in Class D1.0 if the µRTM does not support a signal function, µRTM side view

REVISION CHANGES AND HISTORY

2010/05 : - Experience: High incompatibility between AMC and µRTM boards due to slightly different Zone 3 pin assignment
-> Zone 3 digital class pin assignment recommendation

2012/01 (Rev.A.1) : - Proposed digital subclasses, which can by dynamically grouped when having a Zone 3 electronic keying
2012/01 (Rev.A.1) : - Proposed common GTP in J30 for all subclasses in case of using only one ADF connector.
2012/01 (Rev.A.1) : - Placed µRTM_CLK1, AMC_CLK) to allow placing synchronization circuits onto the AMC or µRTM board.
2012/06 (Rev.A.1) : - ps-stable RESET signal introduced to reset divider phases after power cuts reproducible on µRTMs.
2012/06 (Rev.A.1) : - INTERLOCK1, INTERLOCK2 were introduced to drive µRTMs with vector modulators for high power applications.
2012/06 (Rev.A.1) : - Power Off quiesce action process using a hot-swap handle µRTM is proposed for transient current protection.

2012/11 (Rev.A.2) : - Input from TEWS (N.Koll), DESY (P.Vetrov), KIT (M.Balzer) ->
-> Class D1.x needs an FPGAs on the AMC side and two three row ADF connectors.
-> Digital and analog class are different classes, which needs no pin or connector compatibility.
-> Simplification of filling order of digital IOs and high-speed links -> GTP removed in J30
2012/11 (Rev.A.2) : - Timing clock AMC_TCLK (splitted from TCLKA) moved to (J30 3cd) and replaces RESET
-> A RESET circuits is µRTM specific and should be used on the µRTM
-> AMC_CLK signal and a course RESET from (P30_IO, P31_IO) provides a local ps-stable RESET option.
-> TCLKA length compensation should be done in the MCH, where they are splitted.
2012/11 (Rev.A.2) : - INTERLOCKx signals renamed to general purpose outgoing signals OUT0, OUT1 (J30 4cd, J30 4ef)
2012/11 (Rev.A.2) : - VADATECH, STRUCK and SLAC agreed to DAC filling sequence starting from (DAC0+, DAC0-)
(+) To reduce signal crosstalk AC, DC channels starts from channel 0 contrary to the DAC filling order.
2012/11 (Rev.A.2) : - Isolation of the output signals is realized for the quiesce action and replaces AMC power off.
AMC_TCK, OUT0, OUT1, OUT2, AMC_CLK1,
GTP0-3_CLK_OUT, GTP4-7_CLK_OUT, GTP8-11_CLK_OUT, GTP12-15_CLK_OUT
-> MMC controls disabling of them via buffers.
-> MMC inform FPGA to disable GTP and P30_IO, P31_IO signals.
2012/11 (Rev.A.2) : - Input from TEWS (N.Koll) -> Reduce number of FPGA CC pins.

2012/12 (Rev.A.3) : - Request from KIT, DESY (P.Vetrov) to be compatible to DAMC2 and all existing RTMs
-> Swap AMC_CLK1, RTM_CLK1signals
-> Add AMC_CLK1, RTM_CLK1 signals with fixed direction to Class D1.0
2012/12 (Rev.A.3) : - Request from TEWS (N.Koll) to simplify FPGA CC pins distribution on Zone 3
-> Define FPGA bank distribution to Zone 3
-> Define filling sequence of primary and secondary CC pins to Zone 3
2013/01 (Rev.A.3) : - Preparation for future FPGA bank voltages for LVCMOS and OC signals
-> Concerns only LVCMOS and OC signals pull-up voltages, LVDS transport s only currents.
-> Introduce an µRTM voltage adjustment mechanism provided by the management via I^2C DAC on the RTM side.
(Similar mechanism to FMC Vita57.1, but without using extra pins on Zone 3)
-> Zone 3 termination, class compatibility and reduced functionalities added.

2013/02 (Rev.A.3) : - BoF Group1 Zone 3 pin assignment (Class recommendation) Rev.A.3. in confirmation status.
-> Software E-keying section removed -> Part of BoF IPMI or MMC.