32 Channel Simultaneous MHz Rate Digitizer ACQ132CPCI

ACQ132CPCI Digitizer Board Specification

32 Channels Simultaneous Input 2 Mega Sample per Second per Channel
10, 40, 65 MS/s 14-bit Flash Converter options
Standard 4X oversampling, with analog anti alias option.
Option for 16X oversampling, 2MS/s output, 16 bit effective resolution.
32MS/s burst mode.
6U CompactPCI Data Acquisition Board.
Flexible Digital I/O Subsystem, PXI backplane clock and trigger routing.
Support for multiple board synchronisation
Gigabit Ethernet, output to front panel. or PCI 2.2 32bit, 33MHz DMA upload
600MHz Intel XScale Microprocessor, 1 gigabyte sample memory
Able to operate as CompactPCI peripheral, system board and standalone.
Compatible with ACQ196 Rear Transition Module RTM for optional AO, DIO.

Description

The ACQ132CPCI board handles mid range Data Acquisition applications requiring high channel density sampling in the low MHz range. The board samples 32 input channels simultaneously with 14 bit resolution at speeds up to 4 MS/s (mega-samples per second) sustained capture to memory.

Oversampling Capabilities.

'C' *Continuous* class card has 4X oversampling and optional analog anti alias filter. 'F' *Filter* class able to operate at sample rates to 32 MS/s, with local 16X oversampling filter yields 16-bit effective performance. 'G' *Gated* class captures data in short repeat transients at very high rates.

Distributed Logic Hardware Architecture

The design uses multiple FPGA devices - one Xilinx Spartan 3 FPGA per group of four channels to provide the maximum possible bandwidth from ADC to memory and to implement DSP features. Intelligent board standard features include programmable triggering, flexible clocking and a host of data management functions. Dedicated, high speed Digital I/O allows multiple boards to be synchronized together for high channel count applications. The board can be configured to acquire data into a large on-board data store of up to 1 gigabyte or to stream the data to a PCI host.

Differential Analog Front End.

Fully differential over-voltage protected analog front end, with two software selectable input voltage ranges. Two high density SCSI-68 connectors are used to route input signals in a compact and economical way.

Gigabit Ethernet On Board

Integrated gigabit Ethernet with connection to front panel - the board can operate as an economical standalone networked appliance

Software System Support

As a networked appliance ACQ132CPCI may be controlled via standard TCP/IP networking via a published interface. For conventional PCI backplane control, D−TACQ supports the Linux Operating System and produces full driver support with source code under GPL. Either control interface provides easy to use, high level text commands, ideal for scripting and high performance binary data transfer.

Part Number	Channels	Max Sample Rates		Comment
ACQ132CPCI-32-02C	32	32c x 2M	16c x 4M	4,2X Oversampling, 2.5MHz AAF opt.
ACQ132CPCI-16-04C	16		16c x 4M	2X Oversampling, 2.5MHz AAF opt.
ACQ132CPCI-32-32F	32	IN: 32c x 32M , OUT: 32c x 2M		16X Oversampling filter, ENOB=16
ACQ132CPCI-32-65G	32	IN: 32c x 65M, gated transients		4K sample transients

Full Order Code: ACQ132CPCI-CC-SP[-RTMy]
CC- channel code (32/16), SP speed code (02/04/32)
RTMy – optional RTM (see options below).

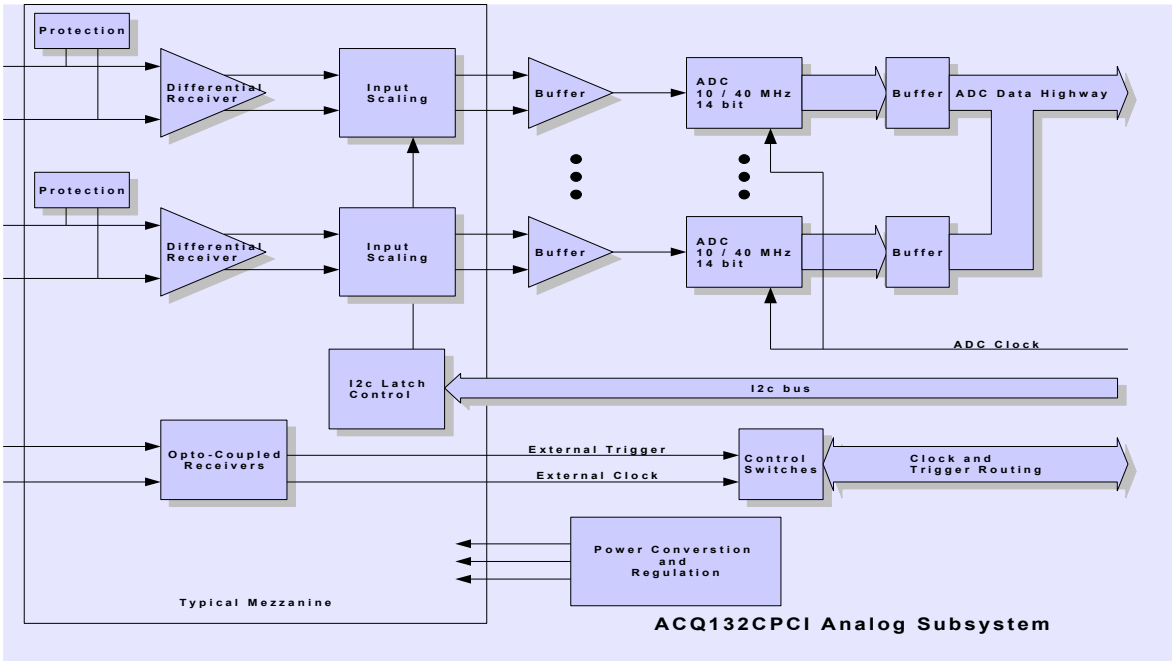
AAF: Anti Alias Filter (analog).
M :MS/s/channel
c : channels

Analog Input Performance (Typical)			
Channel Count	32/16 Simultaneous.	**SINAD**	72 dB * [78db ^{OS}]
Throughput	2/4 MS/s [128MB/s] sustained	**SFDR**	85 dBc *
Resolution	14 bits	**SNR**	72 dB* [78db ^{OS}]
Coupling	DC, Differential Input	**THD**	>-80 dB
Impedance	100K, 20K (^{R1,R2})	**Full Power BW**	2.5MHz
Voltage Ranges	±2.5V , ±10V (^{R1,R2}) Soft Select.	**Small Signal BW**	2.5MHz
Offset Error	0.1% [^{N}]	**Crosstalk (3 dB)**	<88 dB *
Gain Error	0.1% [^{N}]	**CMRR**	>60dB *
INL	2 LSB	[^{N}] by numeric compensation. (^{R1,R2}) Range1,Range2	*1MHz FS input ^{OS} 5X oversampling
DNL	1 LSB		
CMR	±3.5V , ±15V (^{R1,R2})		
Front Panel	***Regular***: 2 x HD68 (16 channels/ connector) or ***LFP*** : Single pin LEMO per channel		

Available RTM types: [Optional] *Uses standard ACQ196CPCI RTM*

RTM1	(100 BaseT Ethernet), console, 6 isolated DI
RTM-DIO32	as RTM1 + DIO32 32 bit programmable Digital IO
RTM-AO16	as RTM1 + AO16 16 x 16bit 2MHz DAC

Analog Input Subsystem Block Diagram:



Digital I/O

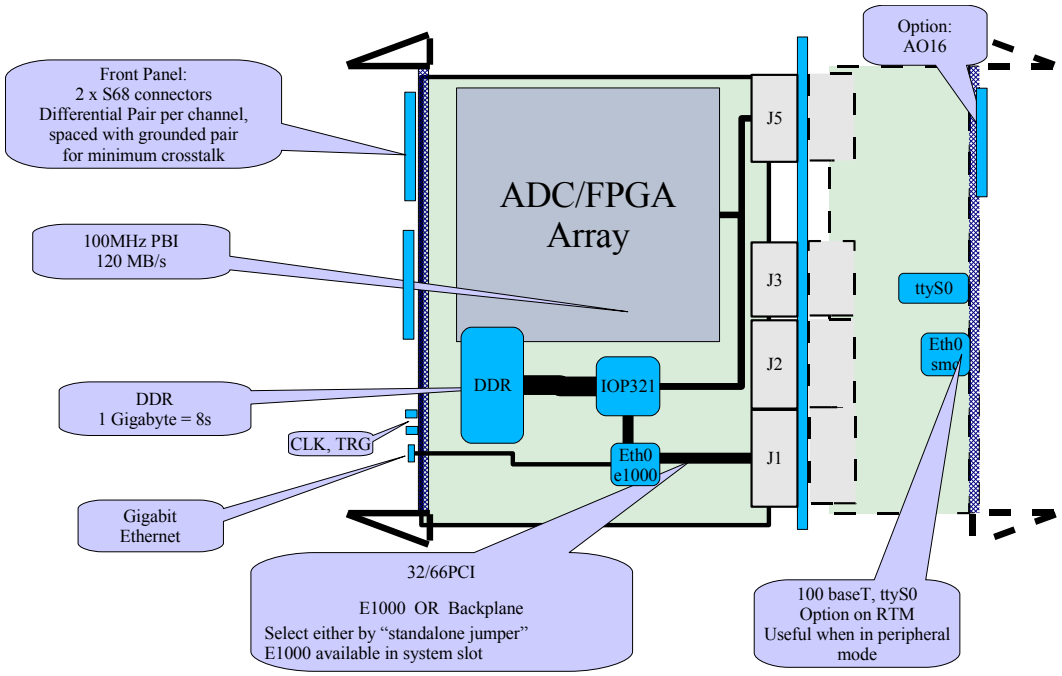
# Dedicated Lines	6
Switching Characteristics	TTL
Front Panel Clock Rate	10MHz max.
Minimum High Time for Trigger	100ns
Minimum Low Time for Trigger	100ns

The Digital I/Os are used for high-speed control including clocks, triggers and multi-board synchronisation , these are available on the Front Panel Rear Panel (via the RTM) or using PXI compatible P2 backplane routing. A low rate front panel clock can be multiplied up by the clock synthesiser.

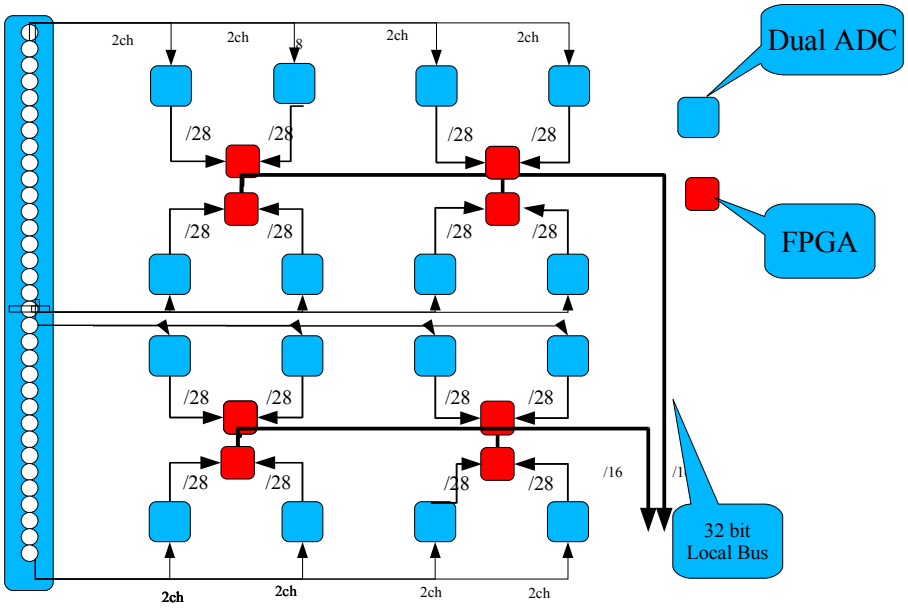
Embedded Computer Subsystem

Processor	600MHz IOP321 Intel XScale Series I/O Processor
FLASH	16 megabyte.
SDRAM	Standard 200 pin DDRSDRAM SODIMM socket for up to 1 gigabyte of memory
PCI Interface	32 bit 33/66 MHz compliant to PICMG CompactPCI Specification 2.0 Rev 3.0
Gigabit Ethernet	RJ45 on front panel. Allows standalone operation, remote control and data upload.
Clock Synthesiser	On Board PLL Clock for creation of sample clock from External or Internal Clock source, output 0.6..40MHz with ~1kHz resolution. Clock Jitter <10ps. optional DDS very high resolution clock.
RS232 UART	Console function accessed via RTM

Physical Layout Concept:



ADC/FPGA Array Layout:



Main Operating Modes

The following paragraphs discuss many of the functions and features of the ACQ132CPCI board. For a complete discussion on the system capabilities please consult www.D−TACQ.com.

Standard Pre / Post Capture Modes

Digital and Analog threshold and edge triggers.
The transient memory is arranged in a circular buffer with data constantly being acquired until the trigger event. Full flexibility of specification of pre-trigger and post trigger data lengths are available for any length up to the limit of available memory.

Generalised Phase Event Mode for maximum flexibility

This allows the user to select a trigger event that is either
A Digital Event or a Software Event
Either Rising or Falling Edge Digital Event
The user sets up a particular event that initiates the pre-trigger phase, then selects another (or the same) event to move to the post trigger phase. This provides maximum functionality in the data acquisition process including support for initial synchronisation events and for “Gated” trigger behaviour in addition to “Edge” trigger behaviour

Repeating Gate Mode RGM

Data capture is gated ON/OFF by external digital signal, data set size is reduced accordingly.
Output data includes a timestamp for each pulse. ACQ132CPCI includes a four bit ***Gate Pulse Generator*** functiony to generate arbitrary streams of pulses, for internal and external use.

Dual Rate Mode DR

Simular to RGM, but capture continues during the GATE OFF period at a lower rate. This allows the average data rate to be reduced, maintaining continuous monitoring, but allowing detail capture during times of interest. This is particularly useful for continuous streaming..

High Throughput Streaming

High Throughput Streaming is available when the system designer can allocate the full PCI bandwidth to the ACQ132CPCI digitizer. In this mode the ACQ132CPCI acting as a Bus Master can continuously stream data at over 200 MBytes/s (64bit 33 MHz PCI), to either host memory or to peripheral storage such as a RAID Disk Array. Reduced Rate Streaming is also possible directly over the local Ethernet.

DMA Upload

D−TACQ provides a high performance DMA upload feature for the captured Transient data. This allows Data to be uploaded over the backplane at high rates.

High Performance FTP upload

Data may be uploaded to the gigabit Ethernet interface using standard FTP protocol at rates in excess of 50MB/s.

In system upgrade

The main logic functions are contained in a FPGA (Field Programmable Gate Array) this is loaded by the Microprocessor at power up from the on-board FLASH Memory. The Microprocessor code is also stored in the FLASH Memory. D−TACQ provides utilities for field upgrade of these FLASH programs allowing feature enhancement to be made in the field without a return to base.

Customisation Potential

Most of the main functions of the ACQ132CPCI can be FLASH upgraded in the field; this allows D−TACQ to produce custom enhancements to the board at low cost without extensive NRE development. Potential areas of enhancement are Real Time signal processing with powerful microprocessor / Xilinx co-processor combination, and fast on-board control loops. Please contact D−TACQ if your application requires functionality that is not currently available.

MDSplus, EPICS, SOAP Web Service on board

ACQ132CPCI supports the MDSplus data archive system, the EPICS distributed control systems and the universal connectivity of Web Services with on-board firmware, making for simplified networked system integration, independent of site OS choices.

Example System Configuration:

1U CPCI chassis, 2 slot, 2 x ACQ132CPCI-32, 64 channels in networked appliance mode.

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