96 Channel Simultaneous Low Cost Digitizer ACQ196CPCI

ACQ196CPCI Digitizer Board Specification

96 Channels Simultaneous Differential Inputs,
16 bit 500 kSPS/channel.

6U, 4HP CompactPCI Data Acquisition Board (single slot)
Flexible Digital I/O Subsystem,
PXI compatible backplane clock and trigger routing
Support for multiple board synchronisation
Intel XScale Microprocessor
Up to 1 GByte of sample memory
PCI 2.2 Interface, 64bit, 66MHz, DMA for max possible PCI bandwidth
96, 64, 32 channels options
Rear Transition Module RTM with 10/100 Ethernet, Digital I/O
RTM with optional 16 channel Analog Output.

Description

The ACQ196CPCI board meets the requirement for high channel density simultaneous data acquisition in cost-sensitve applications. The board samples 96 input channels simultaneously with 16 bit resolution at sample rates up to 500kSPS (kilo-samples per second) per channel, while still offering a robust buffered differential front end input stage with good AC and DC performance.

Hardware Architecture

The design uses a high performance Xilinx Spartan 3 FPGA to provide an efficient data path to the the Intel XScale microprocessor. This board offers the advanced features expected of an intelligent board including programmable triggering, flexible clocking; and a host of data management functions. Dedicated, high speed Digital I/O allows multiple boards to be synchronised together for high channel count applications. The ACQ196CPCI's on board intelligence frees the host processor from complex real time design issues, allowing industry standard operating systems to be used in high performance applications. The board can be configured to acquire data into a large on-board data store of up to 1 GByte or to stream the data to an external PCI device. The FPGA features an array of hardware multipliers, suitable for applications such as FIR digital filtering.

Software System Support

As a networked appliance, ACQ196CPCI may be controlled via standard TCP/IP networking via a published interface. For conventional pci backplane control, D−TACQ supports the Linux Operating System and produces full driver support with source code under GPL. Either control interface provides easy to use, high level ascii commands, ideal for scripting and high performance binary data transfer. The onboard embedded system runs Linux 2.6 tuned for the ARMV5 architecture, and the kernel source code is also available to customers on request. The open source embedded system in combination with the high bandwidth data path offers enormous scope for application customisation. Support for FPGA DSP functionality available subject to support contract.

Typical Systems

Maximum Channels: conventional Pentium hosted 8 slot Chassis, up to 7 ACQ196CPCI boards in peripheral mode for up to 672 channels per chassis. 1200+ channels possible in a 14 slot bridged backplane chassis

Lowest cost, least space: 1U high, 2 x 6U slot chassis, with 2 ACQ196CPCI boards in standalone mode, avoids cost and heat load of a conventional Pentium system board, uses standard Ethernet networking to form a compact, robust, disk less self-contained data acquisition system: 192 channels in 1U!

Ordering Information

Channels	500kSPS/channel
96	ACQ196CPCI-96-500-RTMx
64	ACQ196CPCI-64-500-RTMx
32	ACQ196CPCI-32-500-RTMx

RTMx: RTM1, RTM1-DIO32 or RTM1-AO16
10K input impedance default (ask factory for options at time of order).

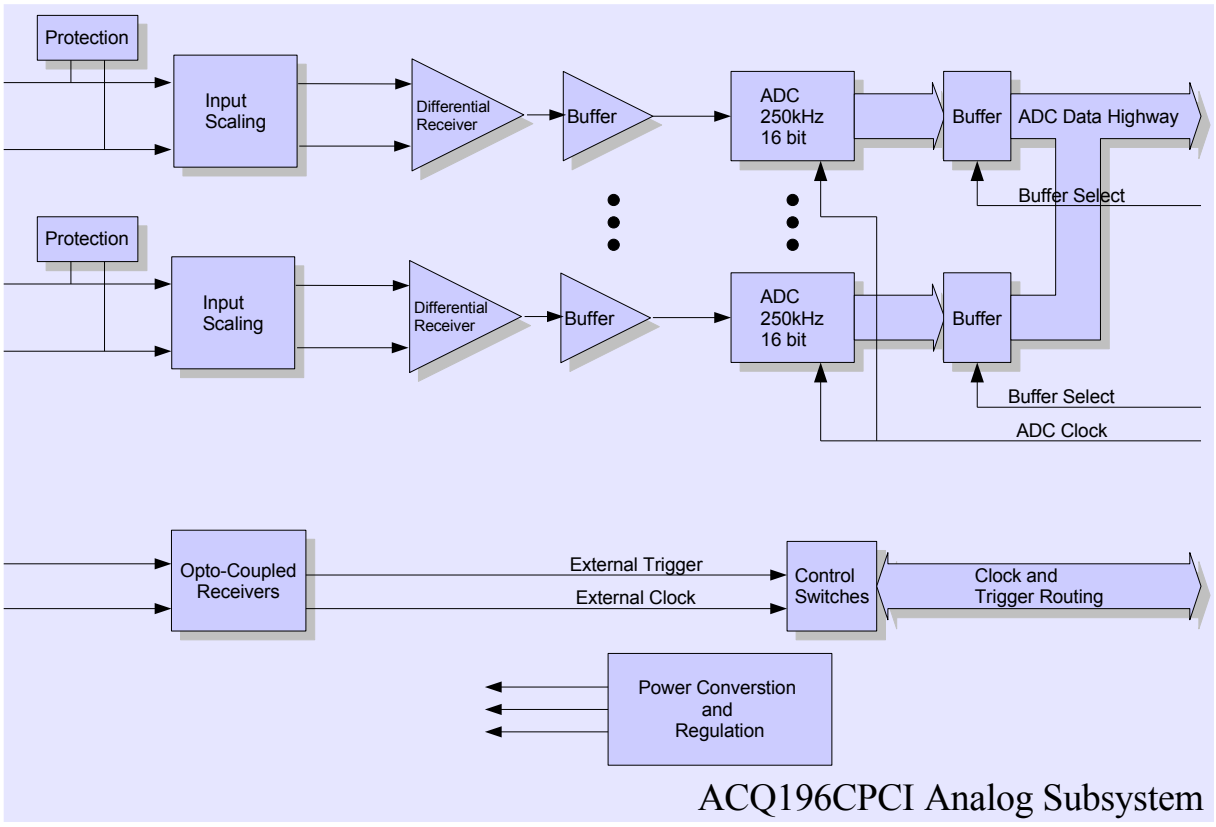
Analog Input Subsystem

Analog Input Performance (Typical)

Number Of Channels	96/64/32		
Throughput	See Ordering Information		
Resolution	16 bits	CMRR	>60dB FS @ 1 kHz
Coupling	DC, Differential Input –	THD	Target >-85 dB
		SINAD	-84 dB*
Sampling	Simultaneous	SFDR	100 dBc*
Input Impedance	20K default	SNR	86 dB*
	100K (factory option)	Full Power BW	250 kHz
Voltage Range	±10V default	Small Signal BW	2 MHz
	±5V (factory option)	Crosstalk (3 dB)	<90 dB @ 1 kHz FS Input
Common Mode Range	±13V	Temperature Stability	<25 ppm/C
Input Voltage Withstand	±100V		
Offset Error	Offset trim to 0.01% FS		
Gain Error	Numerical adjust to 0.01% FS		
INL	± 3 LSBs		
DNL	± 1 LSB		

* *Typical values measured at full scale with a 9.76kHz input.*

Analog Input Subsystem Block Diagram:



Digital Control Subsystem

Digital I/O

Number	6	Digital Expansion Bus
Switching Characteristics	TTL	32 Bit Peripheral Bus for Rear Transition Panel
Maximum Clock Rate	1 MHz	Based Peripherals
Minimum High Time for Trigger	100 nS	
Minimum Low Time for Trigger	100 nS	

The Digital I/Os are used for high-speed control including clocks, triggers and multi-board synchronisation , these are available on the Front Panel (2 signals available) , Rear Panel (via the Rear Transition Board) or using PXI compatible P2 backplane routing.

Processor Characteristics

Processor	IOP321 Intel XScale Series I/O Processor
FLASH	8/16 MBytes
SDRAM	Standard 200 pin DDR SDRAM SODIMM socket for up to 1 GByte of memory, 256 MBytes fitted as standard
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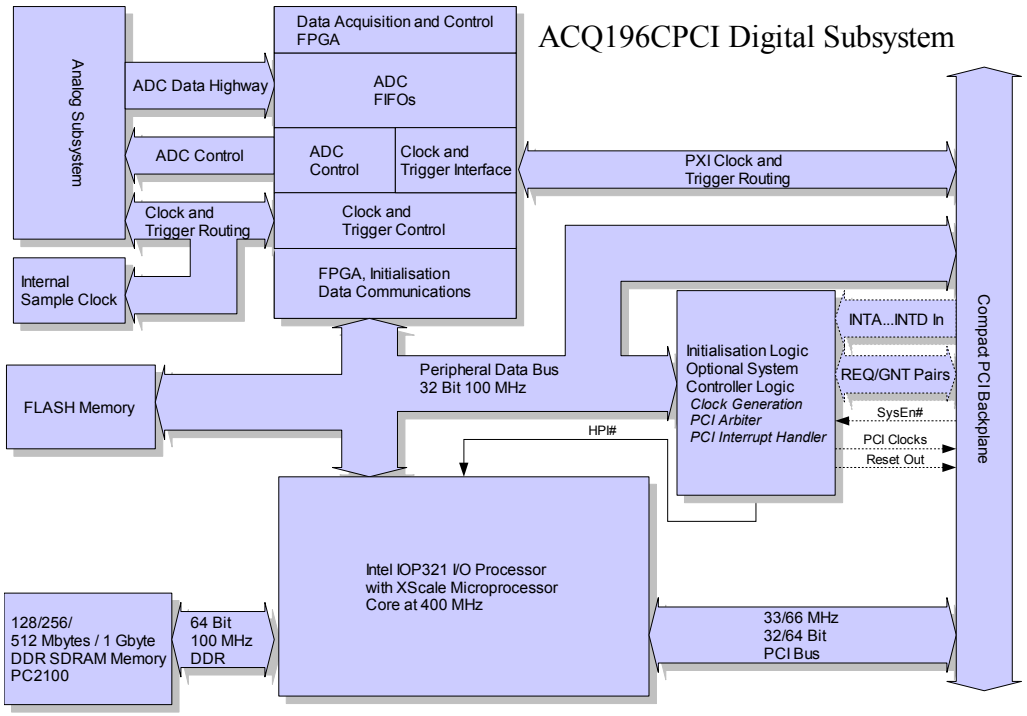
PCI Interface	32/64 bit 33/66 MHz compliant to PICMG CompactPCI Specification 2.0 Rev 3.0. The ACQ196CPCI can be configured as a System Slot Master (System Controller) this allows the board(s) to be used in a standalone mode with no need for a host CPU. When this option has been ordered the board will auto configure for System Slot / Peripheral Slot operation.

Peripherals

An on board Clock Generator is available for the creation of the sample clock from either an External or the Internal Clock source.

Rear Transition Module options:

RTM1:	Ethernet, console, 6 isolated DI lines.
RTM1-DIO32:	As RTM1 + 32 DIO lines
RTM1-AO16 :	As RTM1-DIO32 + 16 channels Analog output.



Digital Control Subsystem Block Diagram

Main Operating Modes

The following paragraphs discuss many of the functions and features of the ACQ196CPCI board. For a complete discussion on the system capabilities please consult www.d-tacq.com.

Standard Pre / post capture modes

Digital and analog threshold and edge triggers.

The transient memory is arranged in a circular buffer with data constantly being acquired until the trigger event. Full flexibility of specification of pre-trigger and post trigger data lengths are available for any length up to the full available fitted memory.

Generalised Phase Event Mode for maximum flexibility

This allows the user to select a trigger event that is either

A Digital Event or a Software Event

Either Rising or Falling Edge Digital Event

The user sets up a particular event that initiates the pre-trigger phase, then selects another (or the same) event to move to the post trigger phase. This provides maximum functionality in the data acquisition process including support for initial synchronisation events and for “Gated” trigger behaviour in addition to “Edge” trigger behaviour

Sub-Sample Streaming Mode

In this mode the board acquires data to a circular buffer as per the Standard Modes but here a sub sample of the data is passed to the host in real time to allow the host to monitor real time data. This is especially useful for mixed control/ diagnostic applications and for more complex “post mortem” evaluation when the decision to move to post capture is determined by the host. The sub sample stream may be made either on the CompactPCI bus or on the local Ethernet if fitted.

High Throughput Streaming

High Throughput Streaming is available when the system designer can allocate the full PCI bandwidth to the ACQ196CPCI digitizer. In this mode the ACQ196CPCI acting as a Bus Master can continuously stream data at at full sample rate on 32bit 33MHz PCI to either host memory or to peripheral storage such as a RAID Disk Array.

Low Latency Mode

In this mode the ACQ196CPCI pushes 1 complete sample worth of memory into host memory to minimise sample latency. This is especially useful in control applications where latency is key. For a typical 32 bit 33 MHz PCI system, all data arrives in host memory in a typical time of less than 12 uS.

DMA Upload

D-TACQ provides a high performance DMA upload feature for the captured Transient data. This allows Data to be uploaded by channel in addition to the entire dataset, sub-sampling DMA is also available.

In System upgrade

The main logic functions are contained in a FPGA (Field Programmable Gate Array) this is loaded by the Microprocessor at power up from the on-board FLASH Memory. The Microprocessor code is also stored in the FLASH Memory. D-TACQ provides utilities for field upgrade of these FLASH programs allowing feature enhancement to be made in the field without a return to base.

Customisation Potential

Most of the main functions of the ACQ196CPCI can be FLASH upgraded in the field; this allows D-TACQ to produce custom enhancements to the board at low cost without extensive NRE development. Potential areas of enhancement are Real Time signal processing with powerful microprocessor / Xilinx co-processor combination, and fast on-board control loops. Please contact D-TACQ if your application requires functionality that is not currently available.

External Connectors

Front panel connectors 3 x 68Way SCSI II sockets for analog signal, 2 x single pin LEMO connectors for external clock and trigger. D-TACQ manufactures a range of compatible signal adapters – Contact D-TACQ Solutions for further information.

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