32 Channel Simultaneous Analog Output Card AO32CPCI

AO32CPCI Simultaneous Analog Output Specification
32 Channels Simultaneous AO 500 kilo Sample per Second per Channel
16-bit DAC Device per channel
Simultaneous Update

Internal, External Clock selection
Internal, External Trigger selection
Optional 64 bit Digital Output DO
Optional Clocked DO
Operating modes, for both AO and DO functions
- Register,
- Arbitrary Waveform Generator AWG
- Low Latency

6U CompactPCI peripheral mode Data Acquisition Board.
PXI backplane clock and trigger routing.
Support for multiple board synchronisation

Description

AO32CPCI provides simultaneous Analog Output (AO) and Digital Output (DO) expansion for CPCI systems. The card provides a lost cost, high performance output expansion for ACQ196CPCI, ACQ132CPCI systems, beyond that provided by RTM-AO16.

AO32CPCI offers substantial performance improvement on RTM-AO16. For AO and DO, there is a FIFO driven AWG function, capable of operating continuously up to 1MHz. ACQ196 is able to drive the AO32 AWG and its own local AI capture concurrently at rates over 100kHz. A single ACQ196CPCI in system slot mode can control up to 7 AO32CPCI cards in a standard chassis.

The AO, DO functions maybe be triggered externally. The card features two separate clock counters, and the both functions may be clocked either by an internal clock, external clock or external divided clock. Clocks and Triggers may be input on the front panel, and/or shared on the PXI-compatible backplane. Apart from AWG applications, the card also allows simple register-per-channel update as well as efficient single cycle low latency update. The later is supported both for extremely low latency Plasma Control System applications, as well as by the general purpose EPICS IOC device support.

Applications:

Plasma Control System PCS

Networked control system elements.

Power Supply control.

Interfacing to existing systems with parallel digital interface.

General purpose AWG applications.

Sonar simulation/stimulation.
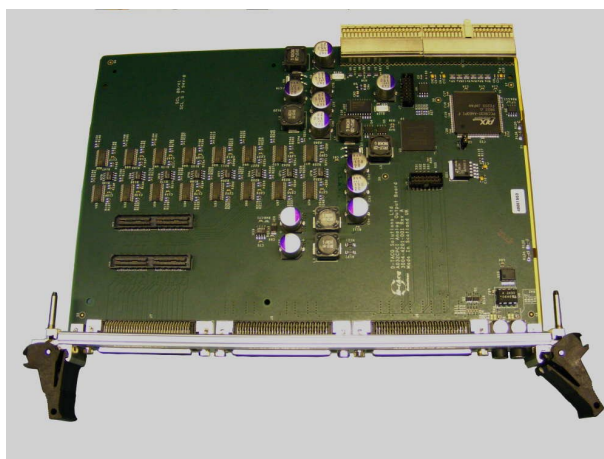
Part Number	AO	DO	Comment
AO32CPCI	32	0	Standard Product
AO32CPCI-DO64	32	64	Standard Product
AO32CPCI-00-DO64	0	64	Special Order only.

Analog Output Performance (Typical)

Number Of Channels	32 Simultaneous.	SINAD	74 dB *
Throughput	500 kS/s [32MB/s] sustained	SFDR	85 dBc *
Resolution	16 bits	SNR	72 dB* [78db OS]
DAC Convert time	1 us	THD	>-80 dB
Output Impedance	10Ω	Full Power BW	2.5MHz
Voltage Ranges	0..10V , ±10V factory select	Small Signal BW	2.5MHz
Offset Error	0.01% [N]	Crosstalk (3 dB)	<88 dB *
Gain Error	1% [N]	CMRR	>60dB *
Output Filter	Single pole, anti-glitch.		
INL	2 LSB	[N] by numeric compensation.	*1MHz FS input
DNL	1 LSB		OS 4X oversampling
CMR	±3.5V , ±15V (R1,R2)	(R1,R2) Range 1, Range 2	

DO64 Option

Number of Bits	64
Logic	TTL, 24mA max drive.
Fastest Update	1usec
Output	Immediate or Clocked
AWG	AWG Capable (with ACQ196 system slot card), unlimited length

Digital Signaling I/O

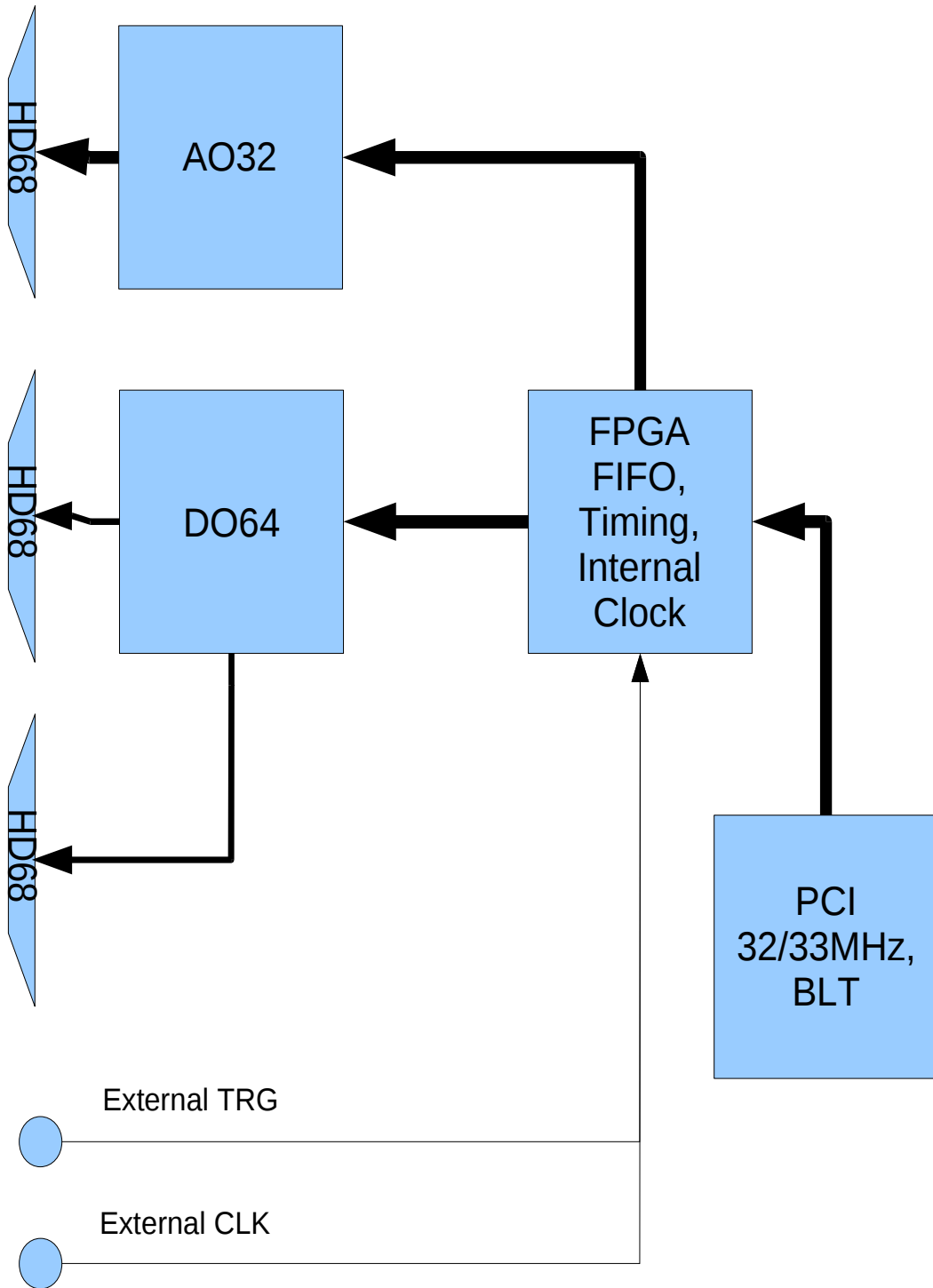|		
# Dedicated Lines	4	The Digital I/Os are used for high-speed control including clocks, triggers and multi-board synchronisation , these are available on the Front Panel Rear Panel (via the RTM) or using PXI compatible P2 backplane routing.
Switching Characteristics	TTL	
Front Panel Clock Rate	2MHz max.	
Minimum High Time for Trigger	100ns	
Minimum Low Time for Trigger	100ns	
Isolation	opto-isolated.	Front panel CLK., TRG inputs only
Clock Divider		Independent divider for each function AO, DO.

Standards Compliance

Formfactor	CPCI 6U PCIMG2.0 rev 3
Bus Interface	PCI 33MHz/32bit, target only, burst capable
Indicator	4 LED lamps
Host Device Driver	Linux 2.6 Driver Provided, GPL

Physical Layout / Block Diagram :

HD68

AO32

HD68

DO64

FPGA
FIFO,
Timing,
Internal
Clock

HD68

PCI
32/33MHz,
BLT

External TRG

External CLK

Registered Operation

Each AO channel is mapped to a 32 bit individually addressable register.

The DO64 word is mapped to two 32 bit individually addressable register.

Output may is updated on software or optional hardware trigger

AWG Operation

All the AO channels are fed with data from a single FIFO buffer.

All the DO channels are fed with data from a separate FIFO buffer.

Host side software services each FIFO, and AO, DO functions may be clocked at different rates.

AO, DO functions are clocked, choice of external front panel, external PXI or internal clocks.

The AO, DO clock inputs each have a programmable divide allowing different rates to be set from a common clock.

Low Latency Operation

In this case, both AO and DO are fed with data from the same FIFO buffer. The FIFO buffer is optimised to transfer data immediately on first sample. The combination of single block write cycle for both AO, DO, and the immediate buffer update is designed for lowest possible latency output.

Example System Configuration:

Networked controller:
1U CPCI chassis, 2 slot,
1 x ACQ196CPCI-96, 96 channels in networked appliance mode.
1 x AO32CPCI-64DO : 32 AO, 64DO in AWG mode.
Typically the ACQ196CPCI will operate as a network controller node running as an EPICS IOC.

Plasma Control System:
Server class Pentium system connects to:
2U CPCI chassis, 4 slot:
1 x PCI bus extender in system slot
1 x ACQ196CPCI-96 in slot 2
2 x AO32CPCI-DO64 in slots 3, 4.
 Here a dedicated algorithm runs on the Pentium. ACQ196 is responsible for transferring data from Pentium host memory to the AO32 devices, and to deliver acquired data direct to the Pentium memory. Such as system is capable of operating dedicated control loops at up to 50KHz.

Sonar Simulation/Stimulation system:
4U CPCI chassis, 8 slot
1 x ACQ196CPCI-96 in system slot
7 x AO32CPCI in peripheral slots
220 channel audio output system. May be used to test large systems based on ACQ196CPCI.