AFHBA404
Host Bus Adapter
Installation Guide

High Performance Simultaneous Data Acquisition

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1 Product Description

1. AFHBA404 is a PCI Express Host Bus Adapter.
2. Provides 4x SFP+ Transceiver ports at up to 6Gbps.
3. Standard PCIe x4 Gen 2.0 card.

1.1 Applications

- High speed control and diagnostics.

1.2 Overview

AFHBA404 provides a high-speed data transfer method to a host PC over fiber-optic SFP+ transceivers.

AFHBA404 includes a standard PCIe x4 Gen 2.0 card-edge connector for interfacing with a host computer.

The AFHBA404 is compatible with D-TACQ standard products including:

- D-TACQ **ACQ2106** : D-TACQ 6 slot *ELF* carrier, Z7030

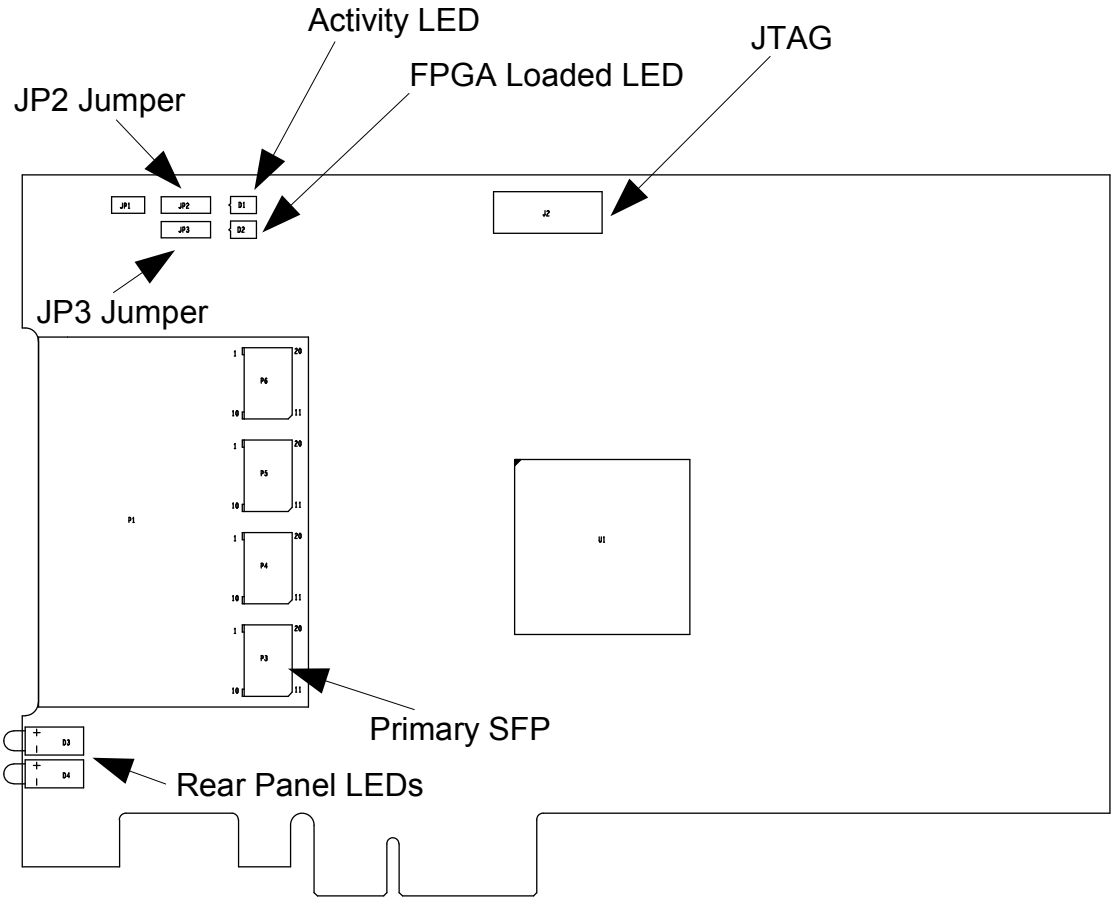
The *FMC/ELF* module standard adds user IO to carrier modules fitted with *FPGA* resource. D-TACQ recommends modules based on the *Xilinx ZYNQ* system on chip, combining *FPGA* resource with a dual-core ARM Cortex A9 and gigabit Ethernet.

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

1.3 Glossary

- *SFP :* Small Form-factor Pluggable
- *PCIe :* Peripheral Component Interconnect Express
- *FMC* : VITA57 FPGA Mezzanine Card.
- Xilinx ZYNQ Soc
- *FPGA* : Field Programmable Gate Array.
- *LPC* : *FMC* Low pin count wiring standard.
- *ULPC* : *FMC* Ultra low pin count (D-TACQ).
- *ULPC+ :* D-TACQ Ultra low pin count with LVDS
- Extended, ELF : *FMC* Extended size module (D-TACQ).
- *CPCI*: Compact PCI

2 Physical Overview



2.1 LEDs

2.1.1 Activity

Flashing Quickly (~2 Hz)	FPGA Running
Flashing Slowly (~1 Hz)	FPGA Running and PCIe Configured

2.1.2 FPGA Loaded

Off	FPGA not loaded
On	FPGA loaded – should light within 20ms of power-on.

2.1.3 Rear Panel

Each LED corresponds to a single SFP+ Port as labelled on the rear panel.

Off	Nothing Connected
Flashing	Fiber Inserted but No Link
On	Link Up

2.2 Jumpers

2.2.1 JP2 – Boot Select

This jumper should not be changed.

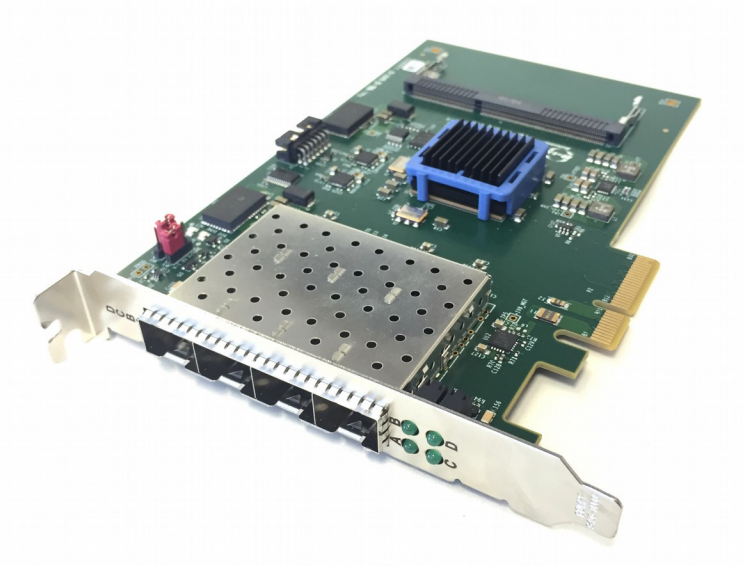
Setting	Description
Fitted 1-2	JTAG Mode
Fitted 2-3 (Default)	SPI Flash Boot (Default)

2.2.2 JP3 – FPGA Bank I/O Voltage Select

This jumper should not be changed from its factory setting.

Jumper	Bank Voltage	Description
1-2	1.8V	Fixes bank voltage for JTAG Flash configuration. This should not be set for DDR3 SODIMM operation.
2-3	1.8V or 1.5V	Voltage is at 1.8V for configuration then drops to 1.5V for DDR3 SODIMM operation at the correct voltage. This should only be set if a DDR3 SODIMM is fitted

2.3 Appearance



2.4 Mating Connectors

AFHBA404 is compatible with standard SFP+ modules such as the Avago AFBR-709SMZ.

3 Specification

#	Parameter	Value
1	Form Factor	Standard PCIe x4 Card
2	Power source	PCIe DC 3.3V, 1.5A
3	Environmental	0°C-40°C Operational -10°C-85°C Non-Operational

4 Changelog

Date	***Rev***	***Section***	***Changes***	***Author***
March 24, 2016	1		Initial release.	Peter Johnston